AIN SHAMS UNIVERSITY
FACULTY OF ENGINEERING
CAIRO-EGYPT

Nanometer Layout Effects on Analog Front End Circuit Design

A Thesis

A thesis submitted in partial fulfillment for the requirement of the degree of Master of Science in Electrical Engineering Electronics and Communication Engineering

Submitted by

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B.Sc. of Electrical Engineering Electronics and Communication Engineering Ain Shams University, 2015

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STATEMENT

This Thesis is submitted to Ain Shams University in partial fulfillment of the degree of Master of Science in Electrical Engineering.

The work included in this thesis was carried out by the author in the department of electronics and communication engineering, Ain Shams University.

No part of this Thesis has been submitted for a degree or a qualification at any other university or institute.

Name : Mohannad Elemam Elshawy
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To My Parents, Sister and Brother

I present to you this thesis to express my deep gratitude and love

Thanks

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Mohannad Elemam Elshawy

Supervised by

ABSTRACT

During the past few years, the concept of integrating multiple applications into a single System-on-Chip (SOC) has occupied a huge segment in the market of integrated circuits. The recent development in this area has led to an increase in the number of Analog/Mixed signal (AMS) components and the functionality that can be integrated per chip. In the digital design flow, the design procedure is captured and the level of automation has been performed easily. On the other counterpart, the AMS design flow suffers from a lack of automation and requires a manual interaction from designer throughout all the design process. Moreover, the design challenges in the advanced nodes beyond 90 nm becomes more significant and tedious for any analog designer. It would be desirable to automate part of the analog design flow (back-end phase) using layout generators to minimize the gap between the front end and back end phases as the layout dependent effects (LDEs) become more significant and tedious for the analog designer in the recent nanometer technology beyond 90 nm.

This work addresses a new analog design methodology that mitigates layout dependent effects (LDEs) on analog circuits. The proposed methodology offers a solution for these effects by minimizing the gap between the electrical and physical design. A layout generator tool is developed and used within the proposed flow. The layout generator tool is parameterized to generate the layout of basic analog building blocks such as Differential Pair and Current Mirror circuits after sizing these circuits in the front end phase by circuit designer. In order to validate the importance of the proposed design methodology, a two stage Miller OTA and a current steering digital to analog converted (DAC) are designed using the

proposed methodology and presented as a case study. All the circuits are designed in 28nm technology and the LDE extraction is done by Calibre-LVS tool to guarantee the accuracy of the extracted data. The developed layout generator tool is used in the design process in order to show the main usage of this tool within the proposed design methodology.

Keywords: Analog Layout Synthesis, Layout Generation, Analog Design, Layout Dependent Effects, CAD

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