Ain Shams University
Faculty of Engineering
Electronics and Communications Department

Simulation of leakage current in nano-scale transistors

A Thesis

Submitted in partial fulfillment for the requirements of Master of Science degree in Electrical Engineering

Submitted by:
Yousry Ibrahim Elmaghraby
B.Sc. of Electrical Engineering
(Electronics and Communications Engineering Department)
Ain Shams University, 2005.

Supervised by:
Prof. Hany Fikry Ragai
Ain Shams University
Prof. Wael Fikry Farouk
Ain Shams University
Dr. Tarek Mohammad Abdul-Kader
Ain Shams University

Cairo 2011

Statements

This thesis is submitted to Ain Shams University in partial fulfillment of the requirements for the degree of Master of Science in Electrical Engineering.

The work included in the thesis was carried out by the author at the Electronics and Communication Engineering Department, Faculty of Engineering, Ain Shams University, Cairo, Egypt.

No part of this thesis has been submitted for a degree or a qualification at any other university or institute.

Name: Yousry Ibrahim Elmaghraby
Signature:
Date:

Curriculum Vitae

Name of Researcher	Yousry Ibrahim Ahmed Mokhtar Elmaghraby
Date of Birth	8-September-1983
Place of Birth	Egypt
First University Degree	B.Sc. in Electrical Engineering
Name of University	Ain Shams University
Date of Degree	June 2005

Acknowledgments

All praise is due to Allah.

I want to thank my supervision committee for their great help and dedication through out the duration of this work. I would like to express my sincere gratitude to Prof. Dr. H. F. Ragaie, for his wise and valuable guidance throughout my work and since my early undergraduate years.

I am in great debt to Prof. Dr W. F. Fikry for supporting and following me up through every tiny step in this work and since my graduation project as well as my professional career.

I am very grateful to Dr. T. M. Abdul-Kader and Eng. Y. M. Sabry for their generous support for all the required technical background through this work starting from the device simulation background, passing by the FETMOSS software description, till the quantum mechanical knowledge and the Green's function.

I would also like to thank Eng. M. O. Darwish for his help in formatting this thesis in LaTeX. And Eng. M. H. Aburahma for his encouragement and advises.

I would also like to thank my colleagues and managers at Silicon Vision for their continuous help and support providing me with the required tools that helped me to complete this work efficiently.

Last, but not least, I would like to thank my family for their constant encouragement, support and patience. I would have never reached this place without their help.

Abstract

As the metal-oxide-semiconductor (MOS) devices in Silicon (Si) Very Large Scale Integration (VLSI) are aggressively scaled down to less than 50 nano meter regime, scaling of the gate dielectric thickness has simultaneously reached as thin as a few nano meters. With decreasing thickness of the oxide layer, the tunneling current through the gate oxide layer increases in a nearly exponential manner. This increase in the leakage current not only detrimentally affects the MOS Field Effect Transistor (MOSFET) performance but also greatly increases the power consumption of the VLSIs, which should be overcome to extend further development in VLSI technologies. Thus, understanding and predicting the tunneling current at high as well as at low bias levels is quite important for the continuous development of advanced nano-scale MOS devices and meaningful Technology Computer Aided Design (TCAD) applications.

The aim of this thesis is to model and simulate the gate leakage current by using a full two-dimensional (2D) non-equilibrium Green's function formalism (NEGF) analysis with open boundary conditions at every electrode (source, drain, top-gate, and bottom gate), which can consider wave nature of electrons in the nano scaled devices coupled with Poisson's equation. The model was implemented into FETMOSS device simulator and results were presented.

Key Words: DG MOSFETs, FETMOSS, Gate leakage current, NEGF, Quantum transport, Real-space.

Contents

Table of contents **V**

List of figures **VIII**

List of tables **XII**

List of symbols and abbreviations **XIV**

1 Literature Review **3**
- 1.1 Introduction to Double Gate MOSFETs . . . 3
  - 1.1.1 MOSFET scaling trend . . . 3
  - 1.1.2 Short channel effects opposing further technology scaling . . . 4
  - 1.1.3 Alternative device structures . . . 6
  - 1.1.4 Overview on the available Multiple-Gate MOSFET structures . . . 7
    - Silicon-On-Insulator (SOI) MOSFETs . . . 9
    - Double-gate SOI MOSFETs . . . 10
    - FinFET SOI MOSFETs . . . 12
    - Surrounding-gate (quadruple-gate) SOI MOSFETs 12
- 1.2 Quantum effects . . . 13
  - 1.2.1 Volume inversion . . . 14

1.2.2 Mobility effects 16
1.2.3 Threshold voltage 17
1.2.4 Quantum Mechanical Tunneling 17
Gate insulator tunneling 17
Source Barrier Tunneling 18
1.3 Tunneling current modeling 19
1.3.1 Distribution Function Modeling 22
1.3.2 Transmission Coefficient Modeling 23
1.4 Device simulation 24
1.4.1 Advantages of device simulation 24
1.4.2 The basic elements of device simulation 26
1.4.3 Numerical solution of semiconductor equations . . 29
Domain and boundary conditions 30
Normalization of semiconductor equations 31
Discretisation of semiconductor equations using Finite difference method 33
1.4.4 Software programming for numerical simulation . 38

2 Double-Gate MOSFETs Simulation Using The Non-Equilibrium Green's Function (NEGF) In Real-Space (RS) 39
2.1 The Non-Equilibrium Green's Function formalism 41
2.1.1 Introduction 41
2.1.2 Retarded and advanced Green's function 42
2.1.3 Green's function calculation 44
2.1.4 Transmission function 48
2.2 The NEGF in Real-Space 49
2.2.1 Introduction 49
2.2.2 Real-Space Hamiltonian matrix for DG-MOSFETs 51
2.2.3 Source and Drain self energies 54

3 Proposed Gate-Leakage Current Model For Double-Gate MOSFETs **61**
3.1 Modified DG MOSFET simulation domain 62
3.2 Real-Space Hamiltonian matrix reformulation 62
3.3 Top/Bottom gate contacts self energies 64
3.4 Terminal current at the Top/Bottom gate contacts 74

4 Results and Discussions **77**
4.1 Introduction to FETMOSS 77
4.2 Device under test structure 78
4.3 Simulation results 81
  4.3.1 Electron density concentration within the device . 81
  4.3.2 Gate current versus Vgs - comparison versus published data 81
  4.3.3 Gate current versus Vgs at different Vds voltage . 83
  4.3.4 Gate tunneling current components versus Vds . . 84
  4.3.5 Gate current versus Vds at different Vgs voltage . 85
  4.3.6 Gate current versus Vds for different Tox 86
  4.3.7 Gate current versus Tox 86
  4.3.8 Gate current versus channel doping concentration . 87
  4.3.9 Gate current versus silicon bulk thickness 88
  4.3.10 Gate current versus gate work function 89
  4.3.11 Gate current versus gate insulator material 91

5 Conclusion **93**
5.1 Summary 93
5.2 Future work 93

References **95**

List of Figures

1.1 2009 ITRS DRAM and Flash Memory Half Pitch Trends. . 4
1.2 Electric field lines in different types of MOSFETs: A: Bulk MOSFET; B: Fully depleted SOI MOSFET, C: Double-gate MOSFET. 6
1.3 Electrostatic Integrity in A: bulk, B: fully depleted SOI, and C: doublegate MOSFETs. 8
1.4 Typical drain-induced barrier lowering in bulk, fully depleted SOI (FDSOI) and double-gate (DG) MOSFETs calculated by MASTAR. 8
1.5 Schematic configuration of CMOS transistors in bulk-Si (left) and SOI (right) wafers 9
1.6 Energy band diagram of (a) bulk, (b) PD-SOI, and (c) FD-SOI 10
1.7 Double-gate SOI device 11
1.8 FinFET structure 12
1.9 Different Surrounding-gate SOI MOSFET structures . . . 13
1.10 Coordinate system and electric field components in a multiple-gate device 14
1.11 Electron concentration profile in double-gate MOSFETs with different silicon film thickness (t_{si}) values. 15
1.12 Mobility versus silicon film thickness in a double-gate transistor. 16

1.13 Gate oxide thickness (nm) versus technology node (nm) . . . 18
1.14 Energy band diagrams illustrating (a) FNT and (b) DT . . . 19
1.15 Tunneling processes in a MOS structure 20
1.16 Comparison of the heated Maxwellian distribution (full lines) with the results from a Monte Carlo simulation (dotted lines) in a turned-on 180 nm MOSFET 22
1.17 The transmission coefficient using different methods for a dielectric consisting of two layers. The shape of the energy barrier and the wave function at 2.8 eV is shown in the inset 25
1.18 The basic elements of semiconductor device simulation . . 27
1.19 Uniform finite-difference mesh 34
1.20 Non-uniform finite-difference mesh 35
1.21 Finite-difference mesh point notation 36

2.1 Conductor of hamiltonian H_C, connected to lead p of hamiltonian H_p 47
2.2 DG MOSFET structure used 50
2.3 Mesh nodes illustration in the simulation domain inside the red frame 52
2.4 The overall system composed of the active device and source/drain contacts 54

3.1 Mesh nodes illustration in the simulation domain inside the red frame that includes the top and bottom gate oxide regions 63
3.2 Illustration for the active device with the extended top gate contact in the y direction 65

4.1 The flow chart of FETMOSS 79
4.2 Device under test structure and parameters illustration . . . 81
4.3 3D Electron density profile at Vds= 0.45V, Vgs= 0.45V . . 82
4.4 Electron density versus device dimensions at x= 10nm, Vds= 0.45V, Vgs= 0.45V 82

4.5 Terminal gate current versus gate to source voltage at 0.0 Volt drain to source voltage 83
4.6 Terminal gate current versus gate to source voltage at 0.0, 0.5 Volt drain to source voltage 84
4.7 Terminal gate current components versus drain to source voltage at 0.6 Volt Gate to source voltage 85
4.8 Terminal gate current versus drain to source voltage at 0.4, 0.6 Volt Gate to source voltage 86
4.9 Terminal gate current versus drain to source voltage at 0.6 Volt gate to source voltage, 0.75nm, 1.00nm gate oxide thickness 87
4.10 Terminal gate current versus gate oxide thickness at 0.6V gate to source voltage, 0.0V drain to source voltage 88
4.11 Terminal gate current versus channel doping concentration at 0.6V gate to source voltage, 0.0V drain to source voltage 89
4.12 Terminal gate current versus silicon bulk thickness at 0.6V gate to source voltage, 0.0V drain to source voltage 90
4.13 Vertical carrier confinement in triangular well in DB MOSFET between the two gates 90
4.14 Terminal gate current versus gate work function at 0.6V gate to source voltage, 0.0V drain to source voltage 91
4.15 Terminal gate current versus different gate insulator material 92

List of Tables

1.1 Normalization constants of physical quantities in the basic semiconductor equations 32

4.1 The simulated devices dimensions, doping concentration, material parameters, simulator options, and FD grid and supply voltage 80