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Dynamic Reconfigurable Hardwired Network-on-Chips

A Thesis

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Abstract

Networks-on-Chip (NoCs) have become the new System-on-Chip (SoC) interconnection scheme. NoC enhanced SoC design to include more complex designs with a greater number of modules, without the need to get into the communication details i.e., intercommunication is separated from computation. NoC provided a flexible design with many topologies, various routing strategies, and switching themes.

In this thesis, we present a dynamic reconfigurable NoC. We combine an adaptive packet switched routing algorithm and a dedicated circuit switching. The dynamic reconfiguration of any link to be used in either packet or circuit switching results in reducing packet latency. Thus, our proposed NoC could carry more traffic than other previous NoC implementations. In the packet switched mode, we have developed a new adaptive routing algorithm for NoC. This algorithm is based on North-Last and South-Last routing algorithms. It classifies a packet based on the location of the destination node relative to the sender node. Switching between the adaptive packet switching and the dedicated circuit switching between any two nodes is done dynamically (i.e., at run time). It is done based on the amount of data to be sent, the type of data, and on the NoC traffic conditions. Switching is done in order to minimize packet latency, while maintaining high throughput, without pre-studying of the SoC application traffic scenario. The proposed NoC has been modeled, implemented in both RTL and TLM, and verified. Simulation results show that, the proposed NoC with the proposed combined switching achieves lower latency that reach 12.5% other FPGA-based NoCs. Also, the combined switching mode can achieve lower latencies, while maintaining dynamic reconfigurability, than other routing algorithms, either static or adaptive.

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List of Abbreviations

ASIC	Application-Specific Integrated Circuit
BFT	Butterfly Fat-Tree
CLB	Configurable Logic Block
DCT	Discrete Cosine Transform
FPGA	Field-Programmable Gate Array
FSM	Finite State Machine
HDL	Hardware Description Language
I/O	Input/Output
LUT	Look-Up Table
NoC	Network-on-Chip
PE	Processing Element
SoC	System-on-Chip
TDM	Time Division Multiplexing
TLM	Transaction Level Modelling
VHDL	VHSIC Hardware Description Language
VOPD	Video Object Plane Decoder

Chapter 1

Introduction

The SoC interconnection using a networking scheme, called Network-on-Chips (NoCs), is a system level design hot topic research. Recently, a special attention was given to routing algorithms and switching schemes (packet or circuit switching) in order to minimize the latency and maximize the throughput.

In this chapter, we give an introduction on the thesis. We show the motivation behind doing this thesis, the contribution, and the organization of the thesis.

This chapter is organized as follows. Section 1.1 presents the motivation behind this thesis. Section 1.2 states the problem targeted and the approach we followed to address this problem. Our main contributions are presented in Section 1.3. Finally, Section 1.4 sketches the organization of the thesis.

1.1 Motivation

NoCs have been widely known as the most flexible, most efficient interconnection methodology for SoCs. This flexibility enabled SoCs to be more complex than ever. However, with higher complexity, more challenges related to quality of service (QoS) appear (e.g., latency, throughput, dynamic reconfigurability, etc.). Many solutions have been previously proposed to enhance the latency and throughput. Adaptive routing algorithms and combined packet and circuit switched mode provide enhancements to NoC QoS. Combined switched mode NoC provides better solutions. However, such solution is harder to

implement than other solutions.

Combined packet and circuit switching mode for NoC has been previously proposed. They are classified as TDM-based NoC [1], or clockless NoC [2]. TDM-based NoC divides a time period T into group of slots. Based on the traffic scenario that will be applied, each slot S is either a shared slot or a dedicated slot. There is a slot table that indicated whether the slot is free or shared. This implies that, there is an effort that should be done to analyze the traffic to make best use of the slots.

The advantage of the dynamic reconfigurable NoC is that it could be employed directly in any SoC directly (i.e., Plug-and-play fashion), while maintaining the minimum packet latency, high throughput, and utilizing the links as much as possible by using such link in either a dedicated path in circuit switching mode, or a shared link in packet switched mode. On the other hand, other combined switching modes require a prior study of the application used, to know the traffic pattern, and adjust the routing parameters to suit the studied traffic pattern. Also, an offline setup of the NoC has to be done to tune the routing parameters. The dynamic reconfigurable NoC eliminates such problem, with the runtime information of the NoC status and the data, any link could be configured to be either a shared or a dedicated link.

We attempt to implement an NoC router that supports both shared and dedicated interconnection. We intend to implement a dynamic reconfigurable NoC that automatically, adapts itself with respect to switching, in run time, without the need to study the traffic pattern of the system applied. By that SoC could be more complex, since the intercommunication is no longer a design problem.

1.2 Problem Statement

NoCs have become the new SoC interconnection scheme. NoC enhanced SoC design to include more complex designs with a greater number of modules, without the need to get into the communication details, i.e., intercommunication is separated from computation. NoC provided a flexible design with many topologies, various routing strategies and switching themes.

Packet switched routing algorithms decide the route to be taken from any source to