Ain Shams University

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Hardware Based Automatic Test Pattern Generation

A Thesis

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Statement

This dissertation is submitted to Ain Shams University for the degree of Master of Science in Electrical Engineering (Computer and Systems Engineering).
The work included in this thesis was carried out by the author at the Computer and Systems Engineering Department, Faculty of Engineering, Ain Shams University, Cairo, Egypt.
No part of this thesis was submitted for a degree or a qualification at any other university or institution.

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Abstract

Automatic Test Pattern Generation (ATPG) is a well known NP-complete problem and has its high importance in digital testing in the Electronic Design Automation (EDA) industry. Accordingly, several types of algorithms have been developed to solve the Automatic Test Pattern Generation (ATPG) problem. Boolean Satisfiability (SAT) techniques have been used to build ATPG algorithms and have had various increments lately including learning and conflict analysis. Much of the performance improvement achieved by state-of-the-art SAT solvers is related to the implementation of conflict analysis which enables the solver to perform non-chronological conflict based backjumping.

Within the context of this thesis, we propose a novel Selective Conflict Directed Jumping (SCDJ) approach for exploring the search space of a given SAT instance. Basically, the proposed algorithm does not need to free the variables that have been assigned in previous decisions made until a conflict has been detected. These decisions are selectively used after conflict analysis to jump deeper into the search space. The proposed Selective Conflict Directed Jumping (SCDJ) scheme is integrated into the latest release of the zChaff SAT-solver and is tested against instances from the DIMACS benchmarks suite. The SCDJ algorithm is also integrated in an ATPG system (SIS) to prove its capabilities in generating test patterns. A hardware-based ATPG solver has been implemented as well using an existing hardware-based Conflict Directed Jumping algorithm through integrating it with SIS.

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ATPG	Automatic Test Pattern Generation
BCP	Boolean Constraint Propagation
BDD	Binary Decision Diagrams
BLIF	Berkeley Logic Interchange Format
BRAM	Block Random Access Memory
CNF	Conjunctive Normal Form
CUT	Circuit Under Test
DPLL	Davis, Putnam, Logemann and Loveland search algorithm
FDA	Failure-Driven Assertions
ISCAS	International Symposium on Circuits and Systems
PDF	Primitive D-cube of Failure
RPG	Random Pattern Generation
RTL	Register Transfer Level

SAT	Boolean Satisfiability
SCDJ	Selective Conflict Directed Jumping
UIP	Unique Implication Points
VLSI	Very Large Scale Integration
VSIDS	Variable State Independent Decaying Sum