AIN SHAMS UNIVERSITY

FACULTY OF ENGINEERING

Electronics Engineering and Electrical Communications

Hardware Accelerator for Robotics and Autonomous Systems (RAS)

A Thesis submitted in partial fulfilment of the requirements of the degree of

Doctor of Philosophy in Electrical Engineering

(Electronics Engineering and Electrical Communications)

by

Hossam Omar Ahmed Omar

Master of Science in Electrical Engineering

(Electronics Engineering and Electrical Communications)

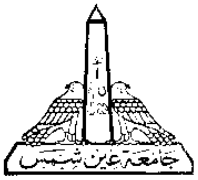
Faculty of Engineering, Ain Shams University, 2015

Supervised By

Prof. Mohamed Amin Dessouky

Dr. Maged Ghoneima

Cairo - (2019)



AIN SHAMS UNIVERSITY

FACULTY OF ENGINEERING

Electronics and Communications

Hardware Accelerator for Robotics and Autonomous Systems (RAS)

by

Hossam Omar Ahmed Omar

Master of Science in Electrical Engineering

(Electronics Engineering and Electrical Communications)

Faculty of Engineering, Ain Shams University, 2015

Examiners' Committee

Name and Affiliation	**Signature**
Prof. Khaled Ali Shehata Electronics and Communications , Arab Academy of Science and Technology	…….
Prof. Mohamed Watheq El-Kharashi Computer and Systems , Ain Shams University	…….
Prof. Mohamed Amin Dessouky Electronics and Communications , Ain Shams University	…….

Date:23 August 2019

Statement

This thesis is submitted as a partial fulfilment of Doctor of Philosophy in Electrical Engineering Engineering, Faculty of Engineering, Ain shams University.

The author carried out the work included in this thesis, and no part of it has been submitted for a degree or a qualification at any other scientific entity.

Hossam Omar Ahmed Omar

Signature

……..…….

Date:23 August 2019

Researcher Data

Name	: Hossam Omar Ahmed Omar
Date of birth	: 01/09/1985
Place of birth	: North Sinai - Egypt
Last academic degree	: Master of Science in Electrical Engineering
Field of specialization	: Electronics and Communications
University issued the degree	: Ain Shams University
Date of issued degree	: 2/2/2015
Current job	: Instructor, Computer Engineering and Technology, American College of the Middle East, Kuwait

Thesis Summary

The swift growth of data size and accessibility in recent years has initiated a shift of philosophy in algorithm designs for artificial intelligence and machine learning, since the ability to learn modern systems and applications automatically from massive amounts of data depending on the conventional algorithms has led to ground-breaking performance in important domains such as natural language processing, Robotics and Autonomous Systems (RAS), speech recognition, and computer vision. Nowadays, the most popular class of techniques used in these domains is called deep learning and is seeing important attention from industry. However, these models require extraordinary massive amounts of data and compute power to train and are limited by the need for better hardware acceleration to be appropriate for scaling beyond current data and model sizes.

While the present hardware acceleration solution has been to use clusters of graphics processing units (GPU) as general purpose processors (GPGPU), the use of field programmable gate arrays (FPGA) or Application Specific Integrated Circuit (ASIC) provide interesting alternatives, since FPGA and ASIC architectures are flexible which give them the ability to explore model-level optimizations beyond what is possible on fixed architectures such as GPUs and CPU hardware based solutions. As well, FPGAs and ASICs tend to provide high performance per watt of power consumption, which is very remarkable for developing large scale server-based deployment or resource-limited embedded applications. Without a doubt, many artificial intelligence and machine learning algorithms are biologically inspired algorithms which mainly depend on dense concurrent computational processing which lead to rely on using FPGA and ASIC as the ideal Platforms for their capabilities to perform Data parallelism, Model parallelism, and Pipeline Parallelism.

In this thesis, we proved that by changing the conventional embedded multiplier blocks and the DSP blocks of the silicon fabric architecture of the FPGA chips we will boost the acceleration capabilities of the FPGA to process any generic Deep Neural Network (DNN) systems while having the ability to have more number of such accelerators due to the optimization level that has been adopted. The four proposed units proved their abilities to exceed the state-of-the-art conventional accelerators by Xilinx and Intel Altera vendors in the computational performance as will be explained in the following chapters. These results have been achieved under two main constrains. The first constrain was the shallow information about the detailed performance features of state-of -the-art DSP block by these manufacturers; and the second constrains is the unavailability of

having a high-technology files to perform a deep testing to the proposed units in order to examine their real performance capabilities. The low power consumption of the proposed units is a clear indication of their promising future to be suitable for critical applications such as the Robotics and Autonomous Systems (RAS).

Key words: Deep learning, convolutional neural networks, computational intelligence, Multiply Array Grid, Multiply Parallel Adder, Pyramidal Neuron Accelerator Architectures (PNAA).

Acknowledgment

All praise and glory go to Almighty Allah who gave me the strength and patience to carry out this work.

First and foremost, gratitude is to the esteemed university, Ain Shams University, and its faculty of engineering members for their high-quality education they supplied me with through my postgraduate studies.

My deep appreciation and gratitude go to my thesis advisors Prof. Mohamed Dessouky, and Dr. Maged Ghoneima, for their constant guidance, support and valuable time they supplied me with through my work in this thesis.

Many thanks and appreciations go to my dear parents, my uncle Sheikh Saleh Abo Khalil and all his family members, my brother and my two sisters for their continuously encouragement and support, and my friends, especially, Mr. Ahmed Hesham, Mr. Ahmed Ashraf, and Mr. Shady Ahmed, for their prayers and Support, they really supplied me with through my postgraduate studies.

August 2019

Table of Contents

List of Figures