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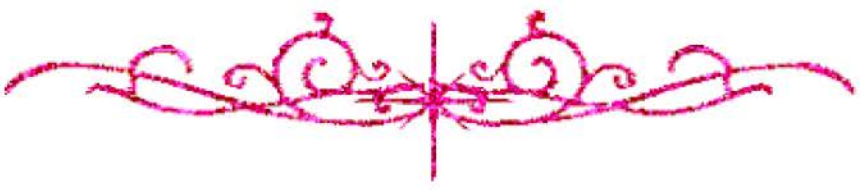

بالرسالة صفحات لم ترد بالأصل

HARDWARE ACCELERATION OF STREAM CIPHER SECURITY ALGORITHMS USING DYNAMIC PARTIAL RECONFIGURATION DPR AND SDSoC TOOLS

By

Sara Taha Mostafa Kamal Taha

A Thesis Submitted to the
Faculty of Engineering at Cairo University
in Partial Fulfillment of the
Requirements for the Degree of
MASTER OF SCIENCE
in
Electronics and Communications Engineering

FACULTY OF ENGINEERING, CAIRO UNIVERSITY
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Title of Thesis:

Hardware Acceleration of Stream Cipher Security Algorithms using Dynamic Partial Reconfiguration DPR and SDSoC

Key Words:
SDSoC; DPR; Stream Cipher; Security; Hardware Acceleration.

Summary:

With the spread of the fourth industry revolution applications which includes many smart devices like Robots, cloud systems, IoT, cyber security...etc, data security has become one of the most important topics that the world are focuses on it due to the huge amount of data that needs to be transferred from point to point on these applications. Data security means protecting data from corruption or from being disclosed from unauthorized users. This thesis presents different implementations techniques to accelerate stream cipher security algorithms which provide both confidentiality and integrity for a variable length of data. The implementation techniques provided in this thesis are implementation using SDSoC tool, implementation using DPR technique and implementation using both SDSoC and DPR at the same time.

Disclaimer

I hereby declare that this thesis is my own original work and that no part of it has been submitted for a degree qualification at any other university or institute.

I further declare that I have appropriately acknowledged all sources used and have cited them in the references section.

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Signature:

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