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ΣΔ Analog-to-Digital Converters
A Thesis

submitted in partial fulfillment for requirements of Master of Science Degree in Electrical Engineering

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To my wife
for her incredible tolerance and support

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Abstract

Ahmed Othman El Shater, "Sigma Delta Analog-to-Digital Converter", Master of Science dissertation, Ain Shams University, 2012.

This thesis presents low-power system and circuit design techniques of high linearity continuous time sigma delta modulator. The target application is analog to digital conversion of wide bandwidths implemented in DSM (deep sub-micron) CMOS technologies. On the system level, a sigma delta modulator with *relaxed analog requirements* is proposed. It is based on the use of multi-bit quantization and a novel feedforward loop filter architecture. This architecture facilitated the use of low gain, power efficient telescopic OTAs (operational transconductance amplifiers) in the loop filter. On the circuit level, a low power implementation of the high linearity input feedforward modulator architecture is proposed with a new clocking scheme that reduces the timing complexity in the feedback path. The implementation eliminated the need for an additional active summer stage without the penalty of signal attenuation due to passive summation. The research also shows that *digitally assisted analog processing* is an attractive low power alternative in DSM technologies, where DEM (dynamic element matching) was used to relax the matching requirements of the feedback DAC capacitors. A power efficient implementation of the DWA (data weighted averaging) algorithm is presented and designed. The aggressive circuit level sizing and analog circuit techniques allow the realization of modulator at low power levels. A top down design methodology was followed to implement the proposed continuous-time sigma delta modulator in a 0.18μm CMOS process. The modulator achieves an ENOB of 13-bit with more than 82dB SFDR over the input bandwidth of 2 MHz at an oversampling ratio of 24X, while consuming a worst case current of 0.77mA from a 1.8V supply for both the analog and the digital parts. This resulted in a FOM (figure of merit) of *45fJ/Conversion*, outperforming the state of the art continuous time and discrete time sigma delta modulators. Key words: continuous-time Sigma Delta modulator, feedforward.

Chapter 1

Introduction

Analog-to-Digital Converters (ADC) are a necessity in all applications that interface with physical signals. They pose as the most challenging block in any application-specific integrated circuit. This thesis aims to implement an ADC utilizing a continuous-time $\Sigma\Delta$ modulator. Continuous-time ADCs claim to support higher bandwidths with lower power than their discrete-time counterparts.

1.1 Motivation

For the past few years, figure-of-merit values below 50fJ per conversion-level have been dominated by successive-approximation converters (SAR), which is attributed to the digital-friendly nature of their architectures. The motive for this thesis is to present a design flow for a continuous-time $\Sigma\Delta$ modulator with an increased focus on aggressively reducing power consumption to break the barrier of 50fJ per conversion-level.

1.2 Outline / Thesis Organization

The thesis is divided into six chapters including lists of contents, tables and figures as well as list of references.

Chapter 1 includes thesis introduction and motivation for choosing a continuous-time $\Sigma\Delta$ modulator as a low power consumption nominee. This chapter ends with the thesis outline.

In Chapter 2, an overview of $\Sigma\Delta$ Analog-to-Digital Converters (ADC) is presented. Basic concepts such as sampling and quantization are explained along with definitions for a number of metrics used to characterize performance of ADCs. $\Sigma\Delta$ ADC architecture is then presented with a discussion of the various factors that affect the performance of $\Sigma\Delta$ ADCs.

In Chapter 3, the system level design of the continuous-time $\Sigma\Delta$ ADC is presented. The target specifications are defined. A systematic approach is followed to select