

# AIN SHAMS UNIVERSITY FACULTY OF ENGINEERING Electronics and Communication Department

## **Design of High Speed Analog to Digital Converter**

#### **A** Thesis

Submitted in Partial Fulfillment for Requirement of Master of Science Degree in Electrical Engineering

**Submitted by:** 

Ramy Said Agieb Said

Supervised by:

Prof. Dr. Hassan Ahmed El\_Ghitani Prof. Dr. Khalid Ali Shehata

Cairo- Egypt

2010

#### **Curriculum Vitae**

Name: Ramy Said Agieb Said

**Date of Birth:** 1/6/1982

Place of Birth: Cairo, Egypt

First University Degree: B.Sc. in Electrical Engineering

Name of University: Shoubra faculty of engineering, Banaha University

Date of Degree: June 2004

#### **Statement**

This thesis is submitted to Ain Shams University for the degree of Master of Science in Electrical Engineering.

No part of this thesis has been previously submitted for obtaining a degree or a qualification before.

Name: Ramy said Agieb

Date : / /

Signature:

#### Acknowledgements

All praise for our god who give us the ability to learn and learn more to grow in the direction of love and happiness for the others and for us.

I wish to express my gratitude to my supervisors, Professor Hassan Ahmed El-Ghitany and Professor Khaled Ali Shehata for their guidance, insightful thoughts, useful discussion, flexibility and encouragement. I have learned a lot from them in both the technical and personal levels .I' am no way capable of appropriately thanking them for their great help.

I deeply indebted for everybody who helped me to complete this work in Modern technology and Information University (MTI) and Ain Shams University.

Finally, I cannot express what's inside me for my parents who worked and worked hard to make from me a good man without anything in return. I just want to say, "I love you" for everything you have done.

## **Contents**

Lis	st of Ta	ables		xii		
Lis	st of Fi	gures		xiv		
Lis	st of S	ymbols		xxiii		
List of Abbreviation						
1	Intro	duction		1		
	1.1	Backgr	ound	1		
	1.2	Motiva	tion	1		
	1.3	Thesis	outline	2		
2	Anal	og to Dig	gital Converter process	3		
	2.1	Genera	ıl parameters	3		
		2.1.1	Resolution	3		
		2.1.2	Quantization Error	5		
		2.1.3	Sampling rate	5		
		2.1.4	Aliasing	7		
	2.2	Static I	Parameters	8		
		2.2.1	Offset and Gain Error	8		
		2.2.2	Differential Non-Linearity Error (DNL)	10		
		2.2.3	Integral Non-Linearity Error (INL)	11		
	2.3	Dynam	nic Parameters	11		
		2.3.1	Signal-to-Noise Ratio (SNR)	12		
		2.3.2	Signal-to-Noise and Distortion Ratio (SINAD)	13		
		2.3.4	Spurious-Free Dynamic Range (SFDR)	13		
	Sumi	mery		15		
3	Anal	og to Dig	gital Converter Architectures	16		
	3.1	Flash A	ADC	17		
		3.1.1	Architecture Detail	17		
		3.1.2	Sparkle Codes	19		

		3.1.3	Metastability	19
		3.1.4	Input Signal Frequency Dependence	20
		3.1.5	Sub-Ranging ADCs	20
	3.2	Pipeline	ed ADC	21
	3:3	Success	sive approximation register (SAR)	25
		3.3.1	Architecture Detail	25
		3.3.2	In-Depth SAR Analysis	27
		3.3.3	DAC	28
	3.4	Integrat	ing ADCs	31
		3.4.1	Architecture Detail	31
		3.4.2	Dual-Slope ADC Architecture	33
	3.5	Sigma-c	delta ( $\Sigma\Delta$ ) ADC	35
		3.5.1	Over all structure and operation	36
		3.5.2	Oversampling	36
		3.5.3	Noise Shaping	39
		3.5.4	Digital and Decimation Filter	42
	Sumn	nary		45
1	Desig	ning the	proposed12-bit pipelined ADC parts	49
	4.1	Archite	cture Details of the pipelined ADC	51
		4.1.1	Operation of a Pipelined Stage	51
		4.1.2	Time Alignment for the proposed pipelined	56
		4.1.3	Digital Correction for the proposed pipelined	56
		4.1.4	Clock Generator for the proposed pipelined	57
	4. 2	_	ng the repeated stage of the pipelined ADC (1.5-bit	57
		4.2.1	SUB-ADC	60
			4.2.1.1 Differential Comparator	61
			4.2.1.1.1 Voltage Comparator	61

				4.2.1.1.2	and Results	62
				4.2.1.1.3	Differential Comparator Simulation and results	76
			4.2.1.2	SUB-ADC	Simulation and results	82
		4.2.2	Sub-DA	.C		91
			4.2.2.1	Sub-DAC	Circuit	93
			4.2.2.2	SUB-DAC	C simulation	93
		4.2.3	Gain sta	ige		93
			3.2.3.1	Concept of	f Bottom-Plate Switching	96
			4.2.3.2	Switch Ca	apacitor Timing	104
			4.2.3.3	Operationa	al Amplifiers	105
				4.3.3.3.1	Operational Amplifier simulation.	107
		4.2.4	Integrati	ion of the 1.	5-bit Stages	112
			4.2.4.1	Simulation	n of 1.5-bit Stage	113
	4.3	Integrat	tion of the	Last stage	of the pipelined ADC	125
		4.3.1	Simulati	ion of the la	st Stage	129
	4.4	Time al	lignments	(shift regist	er) block design	139
	4.5	Design	ing the Co	orrection Lo	gic block	140
	4.6	Two-pł	nase non-c	overlapping	clock	142
		4.6.1	Designin	ng the Clock	k Generator	143
		4.6.2	Simulati	ion Results	of the clock generator	143
	Sumn	nery				147
5	Integr	ration of	the pipeli	ned Analog	to Digital Converter	148
	5.1	Integration of the 4-bit pipelined ADC				
		5.1.1	_		alignment (shift register) for 4-bit	149
		5.1.2	Integration pipelined		gital Correction for the 4-bit	150
		5.1.3	Simulation	on of the 4-b	oit pipelined ADC	151

5.2 Integration of the 12-bit pipelined ADC			166	
	5.2.1	Integration of the Time Alignment (Shift Register) for 12-bit pipelined ADC	167	
	5.2.2	Integration of the digital correction for 12-bit pipelined ADC	167	
	5.2.3	Simulation and Results of the 12-bit pipelined ADC	174	
Sumi	mery		177	
Conclusion				
Future Work				
References1				
Appendix A: Matlab programs used to calculate Static and Dynamic parameters				
Appendix B: Transistors parameters of the UMC 0.13um technology 19				

#### List of abbreviations

A/D Analog / Digital

AC Alternating Current

ADC Analog to Digital Converter

ADSC Analog to Digital Sub Converter

CCD Charge Coupled Device

CMFB Common Mode Feed Back

CMOS Complementary Metal Oxide Semi Conductor

CMR Common Mode Rejection.

DAC Digital Analog Converter

DC Dynamic Characteristics

DLE Differential linearity

DNL Differential Non Linearity

DS-ADC Dual slope -ADC

DSP Digital Signal Processing

ENOB Effective Number Of Bits

Fast Means lower threshold voltage, higher leakage and driving

current.

FF Fast n-ch MOSFET and Fast p-ch MOSFE

FNSP Fast n-ch MOSFET and Slow p-ch MOSFET

FFT Fast Fourier Transform

FSR Full Scale Range

GBW Gain Bandwidth

HDTV High Definition Television

INL Integral Non-Linearity

LCD Liquid crystal display

LED Light Emitting Diode

LSB Least Significant Bit

MDAC Multiplying Digital to Analog converter

MHz Mega Hertz

MSB Most Significant Bit

MSps Mega samples per second.

NMOS Metal Oxide Transistor N-type

OTA Operational Transconductance Amplifier

PDA Personal Digital Assistant

PSR Power Source Rejection

RMS Root Mean Square

RSD Redundant Sign Digit

S/H Sampled / Hold

SAR Successive Approximation Register

SC Static Characteristics

SFDR Spurious Free Dynamic Range

SS Slow n-ch MOSFET and Slow p-ch MOSFET

Slow Means higher threshold voltage, lower leakage and driving

current.

SNFP Slow n-ch MOSFET and Fast p-ch MOSFET

SINAD Signal to Noise And Distortion Ratio

SNR Signal to Noise Ratio

T/H Track/Hold

THD Total Harmonic Distortion

XDSL Digital Subscriber Line –"x" signifies that there are various

flavors of DSL

# List of Figures

Figure 2.1	Values of analog input and output code	4
Figure 2.2	Value of error as function of LSB	4
Figure 2.3	Values of analog input and output code (modulated LSB)	6
Figure 2.4	Value of error as function of LSB (modulated LSB)	6
Figure 2.5	Amplitude distortion caused by aliasing	7
Figure 2.6	Staircase transfer function of an ADC	9
Figure 2.7	Offset and gain errors	9
Figure 2.8	Differential non-linearity errors (DNL)	10
Figure 2.9	Integral non-linearity errors (INL)	12
Figure 3.1	Flash ADC architecture	18
Figure 3.2	Sub-ranging ADC architecture	21
Figure 3.3	Pipeline ADC architecture	23
Figure 3.4	Latency in 4-bit pipeline ADC	24
Figure 3.5	Latency in 12-bit pipeline ADC	24
Figure 3.6	SAR ADC architecture	26
Figure 3.7	SAR operation (4-bit ADC example)	26
Figure 3.8	SAR ADC with Capacitive DAC (16-bit example) [Maxim3 01, Oh 07]	28
Figure 3.9	Single-slope architecture	31
Figure 3.10	Integration time of a single-slop with input voltage	32
Figure 3.11	Dual Slope Integrating ADC	32
Figure 3.12	Dual Slope ADC Integrator Output Waveforms	33
Figure 3.13	Sigma-Delta ADC architecture	37
Figure 3.14	FFT diagram of a multi-bit ADC with a sampling frequency"FS"	37
Figure 3.15	FFT diagram of a multi-bit ADC with a sampling frequency "kF.	38

Figure 3.16	Effect of the digital filter on the noise bandwidth	38
Figure 3.17	Block diagram of a Sigma-Delta modulator	40
Figure 3.18	Affect of the integrator in the sigma-delta modulator	41
Figure 3.19	Effect of the digital filter on the shaped noise	41
Figure 3.20	Relationship between order of sigma-delta modulator and the amount of over sampling necessary to achieve a particular SNR	42
Figure 3.21	Digital side of sigma-delta modulator	43
Figure 3.22	Decimation does not cause any loss of information	43
Figure 3.23	Tradeoff between decision cycles and comparators	45
Figure 3.24	Architecture tradeoffs (components matching with resolution)	46
Figure 3.25	Architecture tradeoffs (Die size with resolution)	47
Figure 4.1	The proposed block diagram for the 12-bit Pipelined ADC	50
Figure 4.2	Switched capacitor MDAC for a 1.5-bit pipelined stage	52
Figure 4.3	Required op-amp GBW as a function of stage resolution [Waltari 02]	55
Figure 4.4	Residue plot of a single bit/stage pipeline ADC, a) Ideal case and b) Real case	58
Figure 4.5	Residue plots of 1.5 bits/stage pipelined ADC ideal case and with comparator offset	58
Figure 4.6	1.5 bit per stage block diagram	59
Figure 4.7	Schematic of the Differential comparator	60
Figure 4.8	Schematic of the Voltage comparator	63
Figure 4.9	Schematic of the biasing circuit for the Voltage Comparator	64
Figure 4.10	Voltage comparator offset (Positive input is less then negative input).	65
Figure 4.11	Voltage comparator offset (Positive input is more than negative input)	66

Figure 4.12	negative input is constant)	67
Figure 4.13	Settling time of Voltage comparator (Positive input increase above negative input)	68
Figure 4.14	Settling time of Voltage comparator output (Positive input decreases below negative input)	69
Figure 4.15	Voltage comparator performance (Differential ramp signal is applied to the two inputs).	70
Figure 4.16	Voltage comparator performance in case of "FF" process variation (Differential ramp signal is applied to the two inputs)	72
Figure 4.17	Voltage comparator performance in case of "SS" process variation (Differential ramp signal is applied to the two inputs)	73
Figure 4.18	Voltage comparator performance in case of "FNSP" process variation (Differential ramp signal is applied to the two inputs)	74
Figure 4.19	Voltage comparator performance in case of "SNFP" process variation (Differential ramp signal is applied to the two inputs)	75
Figure 4.20	Differential comparator offset (Positive input is less then negative input)	77
Figure 4.21	Differential comparator offset (Positive input is more than negative input)	78
Figure 4.22	Differential comparator performance (Differential ramp signal is applied to the input)	79
Figure 4.23	Differential comparator performance (Differential sin-wave is applied to the input at 3.1 MHz)	80
Figure 4.24	Differential comparator performance (Differential sin-wave is applied to the input at 50 MHz)	82

Figure 4.25	range.(a) General range (b) 480 mV input range	83
Figure 4.26	SUB-ADC performance (Differential ramp signal is applied to the input)	84
Figure 4.27	SUB-ADC performance (Differential sin-wave is applied to the input)	85
Figure 4.28	SUB-ADC performance in case of "FF" process variation (Differential ramp signal is applied to the input)	87
Figure 4.29	SUB-ADC performance in case of "SS" process variation (Differential ramp signal is applied to the input)	88
Figure 4.30	SUB-ADC performance in case of "FNSP" process variation (Differential ramp signal is applied to the input)	89
Figure 4.31	SUB-ADC performance in case of "SNFP" process variation (Differential ramp signal is applied to the input)	90
Figure 4.32	Schematic of the SUB-DAC	94
Figure 4.33	Schematic of the Inverter	94
Figure 4.34	Schematic of the 3-input NAND gate	95
Figure 4.35	SUB-DAC performance	97
Figure 4.36	A trace for the SUB-DAC results	98
Figure 4.37	A trace for the SUB-DAC results In case of "FF" process variation	99
Figure 4.38	A trace for the SUB-DAC results In case of "SS" process variation	100
Figure 4.39	A trace for the SUB-DAC results In case of "FNSP" process	101

Figure 4.40	A trace for the SUB-DAC results In case of "SNFP" process	
	variation	102
Figure 4.41	Concept of bottom plate switching	103
Figure 4.42	Schematic of the Gain stage	103
Figure 4.43	Schematic of the full differential OTA	107
Figure 4.44	Schematic of the wide-swing cascode bias circuit	108
Figure 4.45	Figure 4.45 Gain versus transistors dimension (M0&M1)	108
Figure 4.46	Gain versus transistors dimension (M10&M11)	109
Figure 4.47	DC open loop gain of an OTA	109
Figure 4.48	DC open loop gain of an OTA In case of "FF" process variation	110
Figure 4.49	DC open loop gain of an OTA In case of "SS" process variation	110
Figure 4.50	DC open loop gain of an OTA In case of "FNSP" process	
	variation	111
Figure 4.51		111
	variation	111
Figure 4.52	Schematic of the 1.5-bit stage	112
Figure 4.53	Output code of the 1.5-bit stage as a function of the input signal	
	range (a) General range. (b) 480 mV input range	113
Figure 4.54	1.5-bit stage performance (Digital Outputs)	114
Figure 4.55	1.5-bit stage performance (Analog Outputs)	115
Figure 4.56	1.5-bit stage performance (Digital Outputs) In case of "FF"	
	process variation	117
Figure 4.57	1.5-bit stage performance (Analog Outputs) In case of "FF"	
	process variation	118