Ain Shams University
Faculty of Engineering
Computers and System Engineering Dept.

Suboptimal Hardware/Software Codesign in Digital Systems

A THESIS

Submitted in partial fulfillment of the
requirements for the degree

Doctoral

Department of Computers and System Engineering

Ain Shams University

Submitted by
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B.Sc. of Electrical Engineering
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2009

Osaka University

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To my Parents, my Wife and my baby Youssof

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In the name of Allah, most Gracious, most Merciful

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Hassan Ali Hassan Ahmed Youness

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Symbol	Declaration
$G(V,E,w,c)$	Task graph (DAG) Directed Acyclic Graph
SL	Schedule Length
sl	Static Level (b-level without edge costs)
bl	Bottom level(the length of the longest path from a node to an exit node)
tl	Top level (the length of the longest path from an entry node to the node)
cp	Critical path (the longest path in the graph)
n	Task number
V	Number of tasks in the task graph
E	Number of edges in the task graph
P	Number of processors in the target system
P_k	Processor number
P_{rt}	Ready time of processor
P_{src}	Source processor
P_{dst}	Destination processor
$Paths$	Number of paths in the task graph
$Path$	The path number
$Levels$	Number of levels in the task graph
$Level$	The level number
CCR	The communication-to-computation ratio
$ST(n_i)$	Start time of node n_i
$FT(n_i)$	Finish time of node n_i
$Pred(n_i)$	Set of predecessors of node n_i