SPEEDING-UP FAST FOURIER TRANSFORM

By

Mohammed Ahmed Elmotaz Bellah Elsayed

A Thesis Submitted to the
Faculty of Engineering at Cairo University
in Partial Fulfilment of the
Requirements for the Degree of
MASTER OF SCIENCE
in
Electronics and Communications Engineering

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Title of Thesis:

SPEEDING-UP FAST FOURIER TRANSFORM

Key Words:
Fast Fourier Transform (FFT); CORDIC; SQNR; Single-path Delay Feedback

Summary:
This work proposes HardWare-Friendly FFT (HW-F FFT): a restructuring of radix-r FFT butterfly in order to achieve less area-time-power product compared with the conventional algorithm. Moreover, HW-F FFT allows the use of the unequal-gain CORDIC types without the need of any compensation after them. In one case study, Single-path Delay Feedback (SDF) pipeline architecture is used. Given the same hardware resources, HW-F FFT achieves a substantial increase in the Signal-to-Quantization Noise Ratio (SQNR) performance. The proposed algorithm offers up to 75 dB SQNR gain compared to the conventional FFT for different radix-r FFT sizes when different CORDICs and complex multiplier sizes are employed. In the same case study, if it is required to maintain a certain SQNR level, HW-F FFT achieves less computational area, up to 40% less, compared with the conventional FFT.

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Dedication

To the beloved ones, who are not here anymore.

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