Ain Shams University
Faculty of Engineering

THE EFFECTS OF NANO-METER PROCESS TECHNOLOGIES ON DIGITAL CIRCUIT DESIGN FLOW

BY

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A Thesis
Submitted to the University of Ain-Shams
In fulfilment of the thesis requirement for the degree of
Doctor of Philosophy in Electrical Engineering

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Ain-Shams
Cairo, Egypt, 2014

AIN SHAMS UNIVERSITY
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ELECTRONICS AND COMMUNCATIONS DEPARTMENT

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Thesis title:

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Submitted by: Mohamed Said Mohamed Abul Makarem

Degree: Doctor of Philosophy in Electrical Engineering.

Thesis Summary

With the continuous development of today's technology, IC design becomes a more complex process. The designer now not only takes care of the normal design and layout parameters as usual, but also needs to consider the process variation impact on the design to preserve the same chip functionality with no failure after fabrication. In the digital domain both timing and power performance of integrated circuits are increasingly affected by proximity effects. Therefore, it is mandatory to take into account such effects during digital cell characterization accurately to capture the process variations and hence generating more precise timing models. The more accurate modeling of all digital cell variations, the less value of defined On Chip Variation (OCV) specifically in recent technologies. Reducing OCV value leads to more relaxed timing constraints and hence, less power, smaller area and shorter design cycle. This work presents a proposal for a design flow to enhance the manufacturability of the traditional standard cell library. The

novel method comprises fully automated proximity-aware techniques to measure timing variations in digital cells. The new proposed flow is examined on 45 nm recent technologies and results indicate a ±6% variation across whole library contexts with respect to mean value. This shows the importance of having a variability-aware method that qualifies the libraries to be adopted for circuit designs.

The thesis is divided into six chapters including lists of contents, tables and figures as well as list of references and one appendix.

Chapter 1

It includes thesis introduction as well as definitions associated with challenges in recent technologies and their effects on circuit performances. This chapter ends with the thesis outline.

Chapter 2

In recent technologies both timing and power performance of integrated circuits are increasingly affected by process variations. OCV variation models the process and environment variations within one chip. Among the OCV variations are stress and lithography variations, these variations become dominant effects impacting the functionality and performance of designs in advanced technologies. One of the main sources of these variations is the proximity effects from neighboring cells, which significantly influence the lithography process and stress variations values. This chapter contains an introduction to the basic sources of proximity effects in recent technologies. Focus is done on mechanical stress, well proximity effects and lithography effects.

Chapter 3

Many researches in academia have been done to study the context-variability and its impact on circuit performance. Some industrial techniques have been developed to find a CAD solution to take into account these effects during design cycle, and hence reducing the on-chip variation (OCV) amount set in the initial phase of physical implementation design cycle. This absolutely leads to achieve more relaxed designs and hence reduce design cycle. This chapter depicts the different techniques currently used in industry to model OCV in digital design flow. Among of them, are marginal OCV, advanced OCV and statistical static timing analysis (SSTA). Then it will present

different context variability-aware techniques proposed in academia and industry. Finally we will cover different cell-level strategies to mitigate context variation impact.

Chapter 4

In this chapter presents a proposal for a design flow to enhance the manufacturability of the traditional standard cell library. The novel method comprises fully automated proximity-aware techniques to measure timing variations in digital cells. The new proposed flow is examined on 45 nm recent technologies and results indicate a ±6% variation across whole library contexts with respect to mean value. Without context awareness, the variations can reach even more which implies taking this effect into account. Context aware characterization is a very important factor for achieving accurate results in cell characterization process. This shows the importance of having a variability-aware method that qualifies the libraries to be adopted for circuit designs.

Chapter 5

This chapter exploits the proposed flow based on predictive model described in earlier chapter to model stress effects and mitigates the design constraints. It shows the need to reduce the guard-bands that might lead to over-constraints the design, where it is normally adds extra cells during different optimization steps to achieve all timing constraints, and hence increases the total core area and power. Physical and timing results of fully digital design are presented in details for both traditional and proposed flows. Results of different post-routing optimization and checks shows more benefits of using the new flow.

Chapter 6

The dissertation ends by conclusions, summary and future work.

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ABSTRACT

Following the aggressive technology scaling trends and the fundamental limits of optical lithography, the gap between the designed layout and the functionality of what is really fabricated on silicon is increasing. As a consequence, performances predicted during the design implementation may significantly differ from post-silicon measurements. Furthermore, with the increasing difficulty in process control in nanometer technologies, manufacturing variations are growing as a percent of feature sizes. The number of variability sources is also growing as the fabrication processes become more and more complex, and the correlation between different variability sources is also more difficult to predict. The parameter fluctuations cause parametric yield loss, i.e., performance degradation, and the fabricated chips do not function as required by specification. Traditionally, the methodology adopted to determine the timing performance spread of a design in presence of variability is to run multiple static timing analyses at different "corners" that include "best-", "nominal-", and "worst-case". This approach is breaking down because finding those corners requires huge amount of runs to catch the exact corner due to extra layout effects due to cell/device proximities. A possible solution to reduce the number of timing analyses is design and verification with extra design margin normally named as on-chip-variation (OCV) It could be handled by existing corner-based design methodologies only by applying different derating factors for data-path and clock-path delay, and/or by introducing uncertainty margins. Therefore, designing for extreme conditions would automatically take care of the nominal case. However, considering the corner values for each electrical parameter may lead to an over pessimistic estimation of the performance.

The scenario with all parameters in their worst-case values has really a minimal probability to happen in practice, and in several cases it cannot happen at all. Another drawback of the worst-case approach is that it does not provide information to designers about the sensitivity to various parameters, which can potentially be very useful in driving the optimization efforts towards a more robust design. In the digital domain both the situation is worst as timing and power performance of integrated circuits are increasingly affected by proximity effects. Therefore, it is mandatory to take into account such effects during digital cell characterization accurately to capture the process variations and hence generating more precise timing models. The more accurate modeling of all digital cell variations, the less value of defined On Chip Variation (OCV) specifically in recent technologies. Reducing OCV value leads to more relaxed timing constraints and hence, less power, smaller area and shorter design cycle. This work presents a proposal for a design flow to enhance the manufacturability of the traditional standard cell library. The novel method comprises fully automated proximity-aware techniques to measure timing variations in digital cells. The new proposed flow is examined on 45 nm recent technologies and results indicate a ±6% variation across whole library contexts with respect to mean value. This shows the importance of having a variability-aware method that qualifies the libraries to be adopted for circuit designs.

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