AIN SHAMS UNIVERSITY

FACULTY OF ENGINEERING

Computer and Systems Engineering

Emulation-based System-on-Chip Verification

A Thesis submitted in partial fulfilment of the requirements of the degree of

Master of Science in Electrical Engineering

(Computer and Systems Engineering)

by

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Statement

This thesis is submitted as a partial fulfilment of Master of Science in Electrical Engineering, Faculty of Engineering, Ain shams University.

The author carried out the work included in this thesis, and no part of it has been submitted for a degree or a qualification at any other scientific entity.

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Abstract

Systems on Chip (SoC) nowadays, have become heterogeneous in nature. They can be composed of a mix of analog and digital components.

In some verification environments, SystemC is used to model the digital components and SystemC-AMS extensions can be used to model the analog components. Later in the verification process, the digital part can be refined to RTL whose software simulation could be quite slow.

As Systems on Chip are becoming more complex, the functional verification of their RTL-level digital components tends to be performed using emulation platforms to verify large designs faster.

In this work, an approach is proposed that enables the interfacing of SoCs' digital and analog components in an emulation environment, where the digital components (at the RTL level) would be running on the emulator, while the SystemC-AMS components would be running on the associated emulator host machine. The difficulty of this interfacing lies in the SystemC-AMS being a timed environment with a time wheel completely decoupled from emulation time. A case study that illustrates the feasibility of the proposed interfacing approach is also presented.

Thesis Summary

Systems on Chip (SoC) nowadays, have become heterogeneous in nature. They can be composed of a mix of analog and digital components.

In some verification environments, SystemC is used to model the digital components and SystemC-AMS extensions can be used to model the analog components. Later in the verification process, the digital part can be refined to RTL whose software simulation could be quite slow.

As Systems on Chip are becoming more complex, the functional verification of their RTL-level digital components tends to be performed using emulation platforms to verify large designs faster.

Co-emulation is a methodology where components or testbenches, written in SystemC, can be used to generate input data to the design running on the emulator as well as to analyse output data received from the design. In this scheme, SystemC components are usually running on a workstation connected to the emulator.

According to the SCEMI (Standard Co-Emulation Modeling Interface) standard, which is the co-emulation standard followed in the industry, the SystemC side must be untimed. This restriction represents a serious constraint if there is a need to model analog components using SystemC-AMS (which is timed) that would need to communicate with the design running on the emulator. Some emulator's manufacturers offer timed SystemC support, however, they warn the user that the timed SystemC timewheel will be completely decoupled from the emulator timewheel.

In this research, we proposed an approach to interface analog components, modeled using SystemC-AMS and running on the co-emulation workstation, with the RTL design running on the emulator and address the synchronization challenges between the different timewheels. A case study has also been implemented to prove the feasibility of the proposed approach.

The thesis is divided into six chapters as listed below:

Chapter 1:

This chapter introduces the problem addressed by the work presented in this thesis, explains the methodology followed and the contribution presented.

Chapter 2:

This chapter gives a brief overview of the SystemC and SystemC-AMS languages and go through the related work in the area of SystemC/SystemC-AMS modeling.

Chapter 3:

This chapter describes the role of co-simulation and co-emulation technologies.

Chapter 4:

This chapter explains the methodology proposed to interface SystemC-AMS with a digital design running on an emulator.

Chapter 5:

This chapter presents a case study that demonstrates the feasibility of the proposed interfacing approach and provides comments on the experimental results obtained.

Chapter 6:

This chapter concludes the work presented in this thesis and goes through the anticipated future work.

Keywords:
SystemC, SystemC-AMS, Emulation, RTL, Simulation, SCEMI, analog, digital, System on Chip, Functional Verification

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