AIN SHAMS UNIVERSITY
FACULTY OF ENGINEERING
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CAD for 3D Integration - Static Timing Analysis (3D-STA)

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STATEMENT

This thesis is submitted to Ain Shams University in partial fulfillment for the degree of Master of Science in Electrical Engineering.

The work included in this thesis was carried out by the author in the Department of Electronics and Communications Engineering, Ain Shams University, Cairo, Egypt.

No part of this thesis has been submitted for a degree or a qualification at any other university or institute.

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English Summary

This work explores enabling existing flow and tools to handle full 3D designs without introducing drastic changes or excessive computations.
It focuses on full 3D design Static Timing Analysis (STA) with routing parasitic for its critical importance in the digital design flow. It proposes and implements an STA framework "3D-STA" that efficiently handles full 3D extracted digital designs, as well as, regular planar ones. It presents details on the Through Silicon Via (TSV) extraction model, connectivity representation and delay calculations.

This thesis is divided into six chapters including lists of contents and figures as well as list of references.

Chapter 1: Includes introduction and thesis motivation. This chapter ends with thesis outline.

Chapter 2: Contains brief on 3D integration, brief introduction to Through Silicon Via structure and fabrication techniques.

Chapter 3: Discusses in details the enabling of CAD tools for 3D integrated circuit design and introduces the challenges for planar CAD tools in handling 3D ICs.

Chapter 4: Discusses in details Static Timing Analysis technique and algorithm for integrated circuits.

Chapter 5: Proposes a simplified electrical lumped model for TSV and how to be introduced in signal path delay.

Chapter 6: Introduces the developed 3D-STA framework and presents the expremental results of processing ISCAS'85 benchmarks.

Chapter 7: Discusses the conclusions and suggestions for Future Work.

Acknowledgment

ALL THE PRAISES AND THANKS BE TO ALLAH

Praise be to Almighty ALLAH for his endless blessings.

It has been an extraordinary journey, yet a challenging one.

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Prof. *Hani Fekry Ragai*

Dr. *DiaaEldin Khalil*

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List of Abbreviations

TSV	Through Silicon Via
STA	Static Timing Analysis
ITRS	International Technology Roadmap for Semiconductors
CAD	Computer-aided design
SPEF	Standard Parasitic Exchange Format
DSPF	Detailed Standard Parasitic Format
GUI	Graphical user interface
Ts	Setup Time
Th	Hold Time
Tp	Period Time
dp	Path Delay
Arr_{min}	Minimum Arrival Time
Arr_{max}	Maximum Arrival Time
Req_{min}	Minimum Required arrival Time
Req_{max}	Maximum Required Arrival Time

ABSTRACT

3D integration presents a paradigm shift that will enable larger cell integration, through the stacking of multiple layers (tiers) using bonding and Through Silicon Vias (TSVs). 3D integration introduces several benefits in delay areas and foot print.

The use of three dimensional chip fabrication technologies has emerged as a solution for the difficulties related to the continuous scaling of bulk silicon devices. Although the technology already exists, it is undervalued and underutilized largely due to the design and verification challenges that a complex 3D design presents.

CAD tools that are capable of dealing with 3D integrated circuits are still under development. In this work a proposed Static Timing Analysis (STA) tool is presented with a new technique to handle effectively 3D integration with minimum modifications. In addition, a proposed simplified lumped model for TSV is also presented and has been inserted into the framework delay calculations.

The proposed 3DIC timing verification tool serves as an efficient mean to perform all setup and hold timing checks, in which the multi-die design will not be transformed to appear as a traditional 2D design in verification purposes.

Chapter 1 Introduction

1.1 Moore's Law and Interconnect Bottleneck

Any digital system is composed of three main components: memory, data path and control logic. The performance in such systems primarily depends on how well these components can perform the required tasks while communicating with each other.

At a lower level the two key factors that determine the overall performance of a digital system are device delay and interconnect delay. One approach to achieve higher performance is by technology scaling.

By scaling, the channel length of the device is reduced. In other words, the charge carriers have to travel smaller distances in order to reach the drain terminal from the source terminal. Scaling reduces the amount of time taken to move charge carriers from source to drain, thus resulting in faster circuits. The voltage required to drive the charge carriers after creating the channel is also reduced. This is significant as it reduces the amount of power consumed by the system.

Reduced device and interconnect delay help to add more components on a single integrated circuit in compliance with Moore's law [1]. According to Moore's law, the number of transistors that can be added to an integrated circuit doubles every two years. Thus technology scaling has been the driving force behind the semiconductor industry to stay in course with Moore's law.

As a result, interconnect which is relatively slow compared to a device in terms of delay, determines the overall performance of an integrated circuit.

Furthermore, the increased functionality due to scaling has led to the scenario where the overall power is dominated by interconnects. Hence, there is a need for new methodology to tackle this problem of interconnect bottleneck.

1.2 Motivation and Background of 3D ICs

As technology scales, the International Technology Roadmap for Semiconductors (ITRS) projecting on-chip communication, will require new design approaches to achieve system-level performance targets.

Aggressive scaling of process technologies has enabled feature sizes to shrink continuously. While the performance of gates has been improving, interconnects have become a major performance bottleneck [2-4], because global interconnects do not scale accordingly with technologies.

Consequently, interconnect has emerged as the dominant source of circuit delay and power consumption. Figure 1-1 shows the delay of metal and global wiring in future generations. It indicates that with technology scaling, gate delay and local interconnect delay decrease, but global delay increases dramatically. Repeaters can be incorporated to mitigate the delay in global wiring, but this will consume power and chip area.

Therefore, the reduction of interconnect delays and power consumption are of paramount importance for deep-submicron designs. Therefore, numerous research efforts are currently devoted to seeking solutions that can overcome the limitation of wiring requirements for present and future chip designs.

While there have been significant interconnect technology improvements over the last few years, such as the use of copper and low-K dielectric, the industry is striving for additional improvements. Three-dimensional (3D) ICs have recently emerged as a promising means to mitigate these interconnect-related problems [5-10]

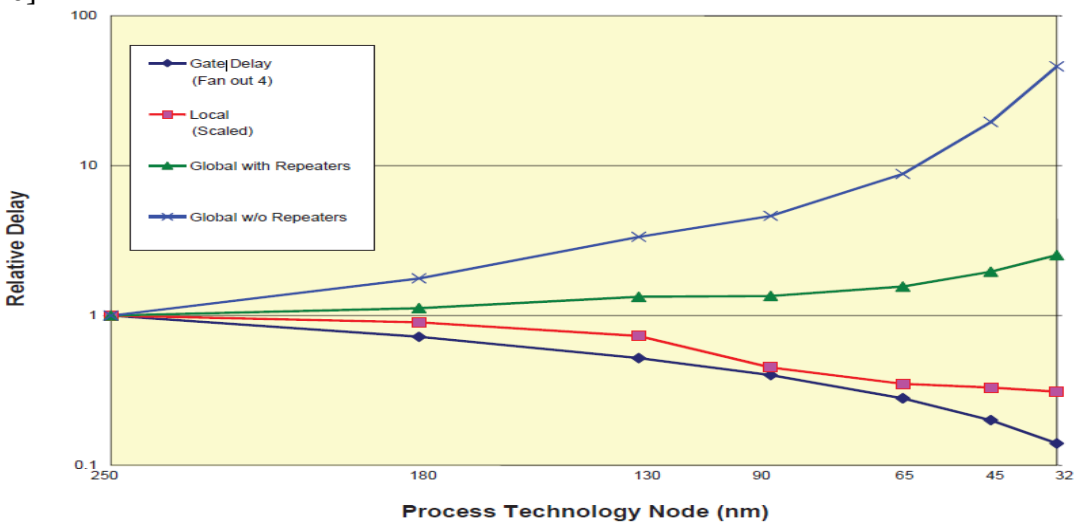

Figure 1-1 Delay for Metal 1 and Global Wiring versus Feature Size (Source: International Technology Roadmap for Semiconductors)