

# AIN SHAMS UNIVERSITY FACULTY OF ENGINEERING

Electronics and Communications Engineering Department

Design Of Wide Band Low Phase Noise Frequency

Synthesizer

submitted by

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A THESIS SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE

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supervised by

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#### Statement

This thesis is submitted to Ain-Shams University in partial fulfillment of the degree of Master of Science in Electrical Engineering.

The work included included in this thesis was carried out by the author in the department of electronics and communications engineering, Ain-Shams University.

No part of this thesis has been submitted for a degree or a qualification at any other university or institute.

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#### Abstract

### Ahmed Farouk Aref Mahmoud, "Wide band Low Phase Noise Frequency Synthesizer", Master of Science dissertation, Ain Shams University, 2008.

This dissertation presents a complete synthesizer chain for the DVB-H standard, which is regarded as one of the most growing standards for wireless consumer applications.

The presented frequency synthesizer presents an innovative fully integrated solution using a newly developed low noise, wide bandwidth LC VCO which uses a new technique for noise cancellation. This technique can decrease the NMOS cross-coupled devices flicker noise injection to the VCO output by 1 to 2 orders of magnitude. This technique can decrease the VCO flicker corner frequency to a maximum of few kilohertz range using standard CMOS technology. This will also results in a a further optimization of the synthesizer power consumption which is a main target for a low power mobile application.

The synthesizer is targeting a wide band of frequencies covering the VHF III band, the entire UHF band and the L-band entitled for DVB-H reception worldwide. The design is targeting a power consumption which is lower than all published work as well as the present market solutions.

A complete frequency synthesizer is presented. Implemented in 0.13um standard process; the synthesizer can have a phase noise of -136dBc/Hz at 1.45MHz offset frequency with a narrow loop bandwidth of 15Khz. The nominal power consumption is less than 30mW with a 1.2V supply. Key words: Phase Locked Loop, PLL, DVB-H, Voltage Controlled Oscillator, Charge pump, Active Noise Isolation.

#### Summary

Over the last ten years digital technology has encouraged a rapid growth in the personal consumption of media. As a result of that new technologies have been developed that enable viewers to watch streamed television-like services on their mobile telephones so that the viewing is no longer limited to the television receiver at home, or in a vehicle, but is widened to allow personalized viewing of television by individuals wherever they are located. In this thesis we developed a wide band low phase noise frequency synthesizer for the DVB-H standard. The work in this thesis is organized as follows:

Chapter 1 is an introduction explaining the motivation for the thesis main subject.

Chapter 2 gives an overview on the DVB-H system from historical and technical point of view, as one of the emerging consumer applications nowadays.

Chapter 3 presents the complete system design steps and all the related simulation results. This includes also the use of a custom made Matlab tool which was used in the system design process. An output of this system design is the performance specifications, different programmable currents and frequency division ratios specified for the synthesizer building blocks described in Chapter 4.

Chapter 4 Shows the circuit level implementation of all of the synthesizer blocks and how these circuits are optimized to achieve the required performance. A detailed description of the newly used VCO with active noise isolation is also included.

Chapter 5 shows all the system integration and verification simulation results. A summary of the synthesizer results as well as a comparison between this work and others related work is also presented.

Appendix A shows the VerilogA code for the different behavioral

blocks used in the semi circuit/behavioral system simulation. Appendix B shows the Matlab code for the developed tool used in the system design.

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