AIN SHAMS UNIVERSITY

FACULTY OF ENGINEERING

Electronics and Communications Engineering Department

Design and Implementation of Moving Target Indicator (MTI)

A Thesis

Submitted in partial fulfillment of the requirements of the degree of

Master of Science in Electrical Engineering

Submitted by

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(Electronics and Communications Engineering)

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STATEMENT

This dissertation is submitted to Ain Shams University for the degree of Master of Science in Electrical Engineering (Electronics and Communications Engineering).

The work included in this thesis was carried out by the author at the Electronics and Communications Engineering Department, Faculty of Engineering, Ain Shams University, Cairo, Egypt.

No part of this thesis was submitted for a degree or a qualification at any other university or institution.

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ABSTRACT

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Clutter is a term used to describe any object that may generate unwanted radar returns that may interfere with normal radar operations like surface clutter (buildings, hills,…) and airborne clutter (chaffs, haze, rain,…). Moving target indicator (MTI) is the most common nowadays technique to overcome the problem of the clutter and fixed targets.

MTI is the process of rejecting fixed or slowly moving clutter while passing echoes from targets moving at significant velocities. In most cases the MTI is sensitive only to radial components of velocity, but area MTI techniques can provide sensitivity to angular components as well.

The main problem that faces the moving target indicator technique is some fixed targets and clutters found on the display camouflage the moving targets , so implementation in the time domain depend on the phase of the fixed targets echo that does not change from pulse to pulse, but the moving targets changes at a rate corresponding to the Doppler frequency.

Fixed targets and clutter cause a great degradation in the radar performance. However a common signal processing in any radar is the moving target indication (MTI). In the other hand, radar having plan position indicator (PPI) needs the delay-line canceller. Processing system in these radars is so massive and complex; since it is supposed to perform a great amount of processing in very short time.

In This thesis, Two new designs of a simple digital moving target indicator (DMTI) using FPGA are developed to overcome processing system problems of radar so we choose the single delay and double delay line canceller for study due to their simplicity in both concept and implementation, But in most radar applications the response of a single canceller is not acceptable since it does not have a wide notch in the stop-band.

A double-delay canceller is an MTI delay-line canceller employing the two-delay-line configuration to improve the performance by widening the clutter-rejection notches, as compared with single-delay cancellers. The FPGA provides flexibility and stability which are important factors in the radar application. In This thesis also a comparison between single and double delay line canceller using MATLAB for software is given. The implementation of a simple digital moving target indicator (DMTI) using FPGA has distinct advantages compared to other application specific integrated (ASIC) circuit for the purposes of this work.

Key words: Clutter, Moving Target Indicator, Doppler Frequency, Field-programmable gate array, Pulsed Radar, ASIC.

SUMMARY

This dissertation demonstrates the importance of implementing Moving Target Indicator using FPGA. The dissertation is in four chapters organized as follows:

Chapter One: It begins with an introduction on the use of MTI technology in RF design.

Chapter Two: In this chapter, clutter model and signal processing techniques and also the background information related to MTI filter are given in this chapter.

Chapter Three: In this chapter, Different configurations of the MTI filters are given along with their frequency response characteristics. The digitalized and delay problem is explained and the staggered PRF MTI filter solution is given the design of two different types of delay line cancellers (MTI) filters are given.

Chapter Four: First, two types of design approaches are presented in relation with delay line cancellers design using software implementation. Second, simulation results for this design where a comparison between simulation and measurement results is included.

Chapter Five: First, the hardware implementation is taken into account for the designed filters. Second, the definition and the properties of FPGA are presented. Then the effect of clutter on the earlier designs is discussed and the results are compared with respect to a number of figures and measurement results is included.

Finally, the thesis ends by extracting conclusions and stating future work that might be done based on this work.

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