FRONT-END ENHANCEMENTS FOR CAIRO UNIVERSITY HARDWARE/SOFTWARE PARTITIONING TOOL (CUPSHOP)

By

Ahmed Hamed Fatehy Hamed

A THESIS SUBMITTED TO THE
FACULTY OF ENGINEERING AT CAIRO UNIVERSITY
IN PARTIAL FULFILLMENT OF THE
REQUIREMENTS FOR THE DEGREE OF
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IN
ELECTRONICS AND COMMUNICATIONS ENGINEERING

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Title of Thesis:
FRONT-END ENHANCEMENTS FOR CAIRO UNIVERSITY HARDWARE/SOFTWARE PARTITIONING TOOL (CUPSHOP)

Key Words:
HW/SW Co-Design, High Level Synthesis; C Front-End; Embedded Systems; Control-Data Flow Graphs; Intermediate Representations;

Summary:
This thesis introduces a Front-End enhancement for Cairo University Particle Swarm optimization Hardware/sOftware Partitioning (CUPSHOP) tool by enabling this tool to accept input designs written in ANSI C. This Front end can accept hierarchical input C codes of arbitrary number of levels. It extracts a corresponding control and data flow diagram (CDFG) representation of the system, together with all the data base information needed to define the design completely. This CDFG is fully compatible with CUPSHOP, and can also be used with several HLS and HW/SW partitioning tools. The developed C front end is tested successfully against several published HLS benchmarks, including benchmarks from CHStone suite.

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Dedication

To my Father, my Mother and my Wife

“THE ENDLESS SOURCE OF SUPPORT IN MY LIFE”

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Nomenclature

ADPCM	: Adaptive Differential Pulse Code Modulation.
ALAP	: As Late As Possible
ASAP	: As Soon As Possible
ASIC	: Application Specific Integrated Circuits
ASIP	: Application-Specific Instruction-Set Processor
CDFG	: Control-Data Flow Graph
CFG	: Control Flow Graph
CFSM	: Co-design Finite State Machine
CPU	: Central Processing Unit.
CUPSHOP	: Cairo University Particle Swarm Optimization HW/SW Partitioning.
DAG	: Directed Acyclic Graph.
DCT	: Discrete Cosine Transform.
DFG	: Data Flow Graph.
DSP	: Digital Signal Processing.
FFT	: Fast Fourier Transform.
FIR	: Finite Impulse Response.
FPGA	: Field Programmable Gate Array.
GA	: Genetic Algorithm.
GUI	: Graphical User Interface.
HCT	: Hierarchal Call Tree.
HW	: Hardware.
IR	: Intermediate Representation.
JPEG	: Joint Picture Expert Group.
KPN	: Kahn Process Networks
LE	: Logic Element.
LLVM	: Low Level Virtual Machine
LUT	: Look-Up Table.
MP3	: MPEG-1 Audio Layer 3.
MPEG	: Moving Picture Experts Group
MPSOC	: Multi-Processor Systems-on-Chip.
MUX	: Multiplexer.
OSCI	: Open SystemC Initiative
PPA	: Pipeline of Processing Arrays
PSO	: Particle Swarm Optimization.
RTL	: Register Transfer Logic.
SDF	: Synchronous Data Flow.
SoC	: System on a Chip.
SW	: Software.
TLM	: Transaction Level Models.
VHDL	: Very high speed integrated circuits Hardware Description Language.

Abstract

The first-release of **C**airo **U**niversity **P**article **S**warm optimization **H**ardware/s**O**ftware **P**artitioning (**CUPSHOP**) tool was previously developed at Cairo University. It accepts Behavioral, Un-Timed, Algorithmic-Level, VHDL, designs representation, with limited set of VHDL commands, and outputs a valid Hardware/ Software partition and schedule for the design subject to a set of area/ power/ delay constraints. This thesis introduces a Front-End enhancement CUPSHOP tool by enabling this tool to accept input designs written in ANSI C. The developed Front end can accept hierarchical input C codes of arbitrary number of levels. It extracts a corresponding control and data flow diagram (CDFG) representation of the system, together with all the data base information needed to define the design completely. This CDFG is fully compatible with the first release of CUPSHOP, and can also be used with several HLS and HW/SW partitioning tools.

The work done in this thesis employs several open-source tools towards building a C-input Front end for CUPSHOP. We invoke Eclipse IDE, an ANSI C editing and debugging tool, for Hierarchical Call Tree (HCT) extraction. We also invoke GAUT, an academic open source High-Level Synthesis tool for extracting Data Flow Graph (DFG) from an input design written as a flat ANSI C code. We also use the MATLAB exchange cementer library to add graph visualization capability to CUPSHOP. Finally, the developed Front-End constructs an internal database of the input design that paves the way for the HW/SW partitioning process and further, for final HDL code generation.

The main functionality of CUPSHOP's C Front-End is to convert input designs written in ANSI C language into CDFG representation. It should be highlighted that the CDFG is fully describing the input design; hence it can provide the required backbone for the HW/SW co-designs partitioning tool CUPSHOP and a High-Level synthesis tool as well.

The developed C front end is tested successfully against several published HLS benchmarks, including benchmarks from CHStone suite.