MODELING OF THE DYNAMIC PERFORMANCE OF MOSFETs USING SPICE

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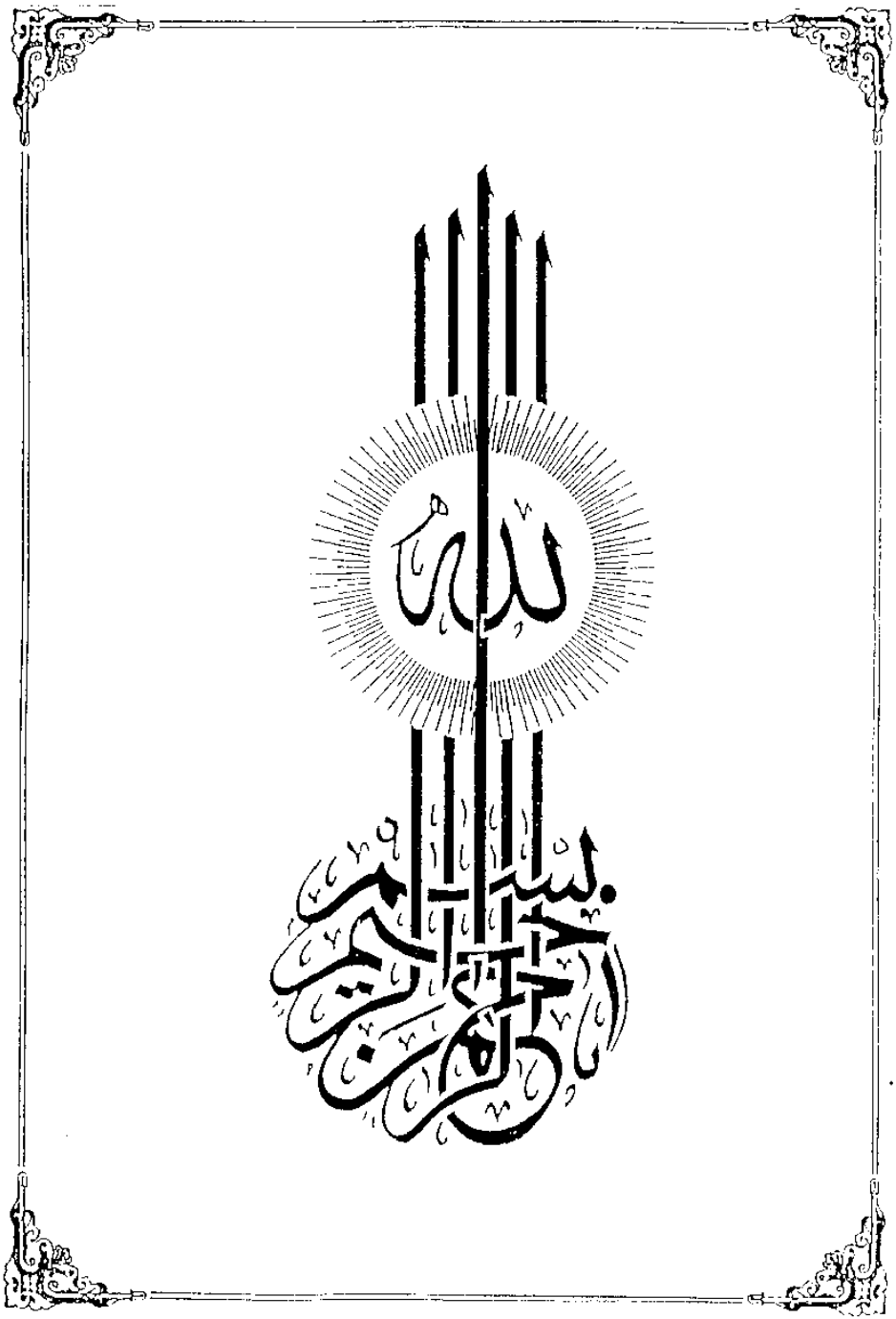

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STATEMENT

This dissertation is submitted to Ain Shams University for the degree of **Master Of Science** in **Electrical** Engineering . The work included in this thesis was carried out by the author in the Department of **Electronics and Computer Engineering** , Ain Shams University, from **November 1989** to **October 1991** . No part of this thesis has been submitted for a degree or a qualification at any other University or Institution.

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MODELING OF THE DYNAMIC PERFORMANCE OF MOSFETS USING SPICE

ABSTRACT

This thesis deals with the modeling of the dynamic performance of MOS devices which constitute the main building block of modern integrated circuits. A distributed equivalent circuit and a novel approach for modeling such devices using the circuit simulator SPICE are proposed in this work. Simulation of uniform channel devices as well as devices with random charge distributions and local damage of the gate oxide has been performed.

Chapter one is an introduction to the theoretical basis of the dynamic performance of MOSFETs. Also, a brief summary of the existing small signal models of MOS transistors is presented and the device parameters related to the dynamic performance are introduced. Finally, a brief description of the circuit simulator SPICE is given.

Chapter two is devoted to the simulation of the dynamic behaviour of devices with uniform charge distributions inside the gate oxide. The channel time constant is simulated for several values of the technological parameters and its dependence on the interface trap density is studied.

Chapter three deals with locally damaged devices as well as those with random interface charge distributions. The simulation approach used to deal with these two problems is presented and the results obtained from the analysis are discussed.

Experimental measurements have been carried out on several devices and their results are presented in chapter four. Comparison to the results of SPICE simulations shows that a very good agreement exists between the experimental and the simulation results indicating that the proposed approach is quite accurate.

Finally, concrete conclusions as well as the proposed directions of future study are indicated.

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Introduction

CHAPTER 2

Simulation Of The Dynamic Performance Of The Uniform MOS Transistor

CHAPTER 1

INTRODUCTION

In this chapter a brief review of the existing small signal models for MOS devices is presented. The basic parameters representing the dynamic behavior of the MOS transistor is presented. Also a brief description of the SPICE program is given along with the A.C. small signal MOSFET model available in SPICE.

1-1 SMALL-SIGNAL MODELS FOR THE MOS CAPACITOR

The small signal equivalent circuit model of the MOS capacitor has been treated in literature in several ways, the transmission-line modeling of MOS capacitors is one of these methods. One of the earliest models for the MOS capacitor was introduced by Lehovec and Slobodskoy [1], their methodology to arrive at an equivalent circuit was to follow step by step the flow of A.C. charges, electrons and holes, from the bulk of the semiconductor to the interface between the semiconductor and the oxide. Each step can be associated with a resistor. Accumulation of A.C. charges can be associated with capacitors, finally, they have reached a lumped circuit model obtained from physical considerations and charge analysis [1].

C.T. Sah et al. [2] have used a small signal expansion of the transport equations, these transport equations can be synthesized to give the complete equivalent circuit of the semiconductor region for one dimensional geometry as shown in Fig.(1.1) where C_o is the oxide capacitance, G_{pst}, G_{nst} and C_{ts} represent the carrier capture conductance and storage

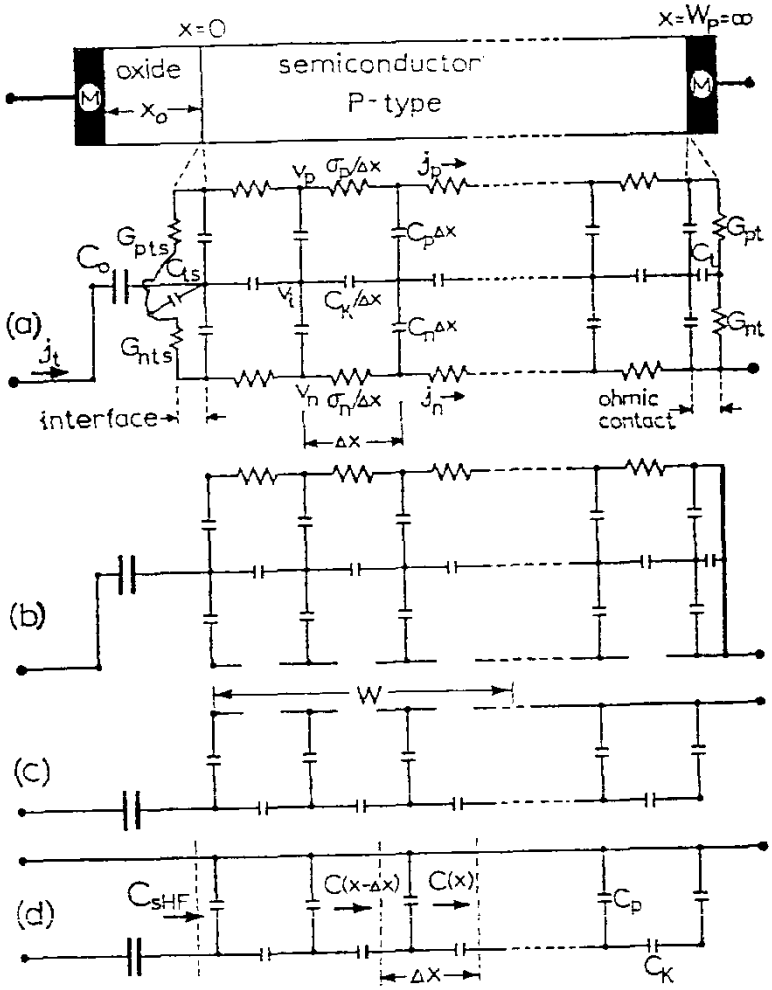


Fig. (1.1). The upper part shows the MOS structure where M is the metal contact. (*a*) The complete equivalent circuit including surface states at $x = 0$ and the ohmic contact at $x = \infty$, but excludes recombination in the bulk. (*b*) The complete high frequency equivalent circuit with an ideal ohmic contact. (*c*) The high frequency equivalent circuit for an inverted surface. (*d*) The high frequency equivalent circuit for a non-inverted surface which is also valid for an inverted surface.

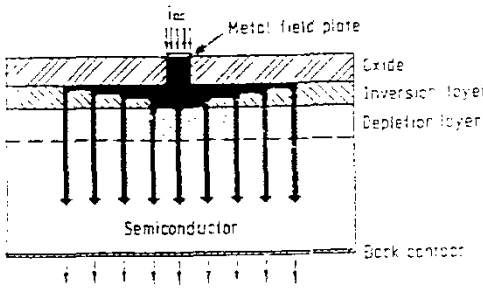


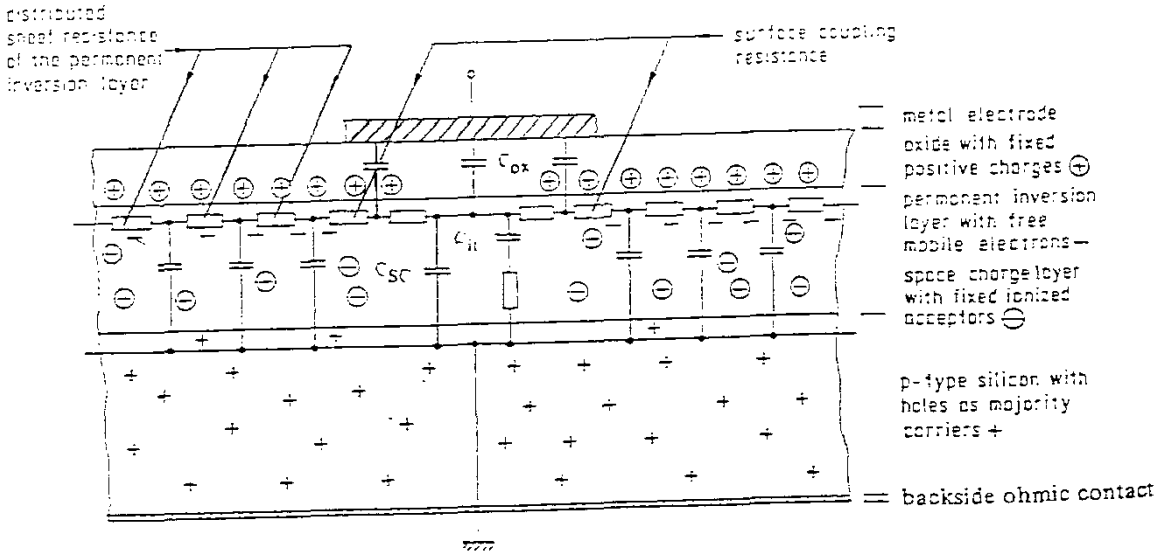
Fig. (1.2) *Representation of how an AC current flows through an MOS capacitor in the presence of an external inversion layer (After Nicollian E.H. and Goetzberger A.*

capacitance at the interface states, and G_{pt}, G_{nt} and C_t those at the ohmic contact. Here $C_p = q^2 p/kT$, $C_n = q^2 n/kT$, $C_k = \varepsilon_s \varepsilon_o$, $\sigma_p = q\mu_p p$ and $\sigma_n = q\mu_n n$. p and n are the static hole and electron concentrations, C_k is the permittivity of the semiconductor, μ_p and μ_n are the carrier mobilities in the bulk.

In the high frequency range, the electron (minority carrier) conductance σ_n is removed since minorities can not be supplied at a sufficiently rapid rate to follow the signal frequency. Thus the equivalent circuit simplifies to that in Fig.(1.1.b). The transmission-line can be further simplified for non-intrinsic surfaces as follows:-for an inverted surface, there is a hole (majority) depletion layer, $0 < x < W$, where $C_p = \sigma_p = p = 0$. In the bulk, $x > W$, σ_p can be shorted if the signal frequency is much less than the dielectric relaxation time of majority carriers, (σ_p/C_k). These considerations are shown in Fig.(1.1.c). For a non-inverted surface, $p \gg n_i$, so that $\omega \ll \sigma_p/C_k$ also in the surface layer $0 < x < W$, giving Fig.(1.1.d). However, since $C_p = 0$ for $0 < x < W$ in the inverted surface case, Fig.(1.1.d) actually represents both the inverted and non-inverted surface conditions.

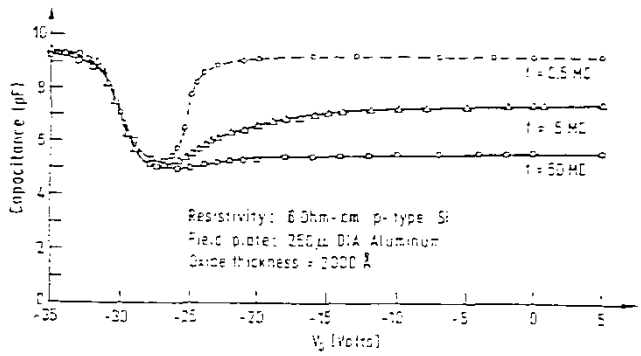
These considerations show that σ_p contributes a large semiconductor conductance only near the intrinsic surface condition where a conductance peak is often observed experimentally. Y.C.Sun and C.T.Sah [3] more recently proposed a one dimensional small signal equivalent circuit of the MOS capacitor very close to that in Fig.(1.1), but including bulk traps, and also a two dimensional small signal equivalent circuit including interface edge effects [3].

These equivalent circuits were considered to be very complex [4] and it is interesting to note that they can be simulated using SPICE, using



- *Equivalent circuit of a MOS structure in the presence of a permanent inversion layer.*
  – Directly below the metal gate, we have a normal MOS capacitor, schematically represented here by C_{ox}, C_{SC} and C_{it}.
  – Beyond the metal gate, the permanent inversion layer forms a transmission line with a low-pass filter characteristic.
  – The intrinsic MOS capacitor and the permanent inversion layer (or channel) are connected by the surface coupling resistor. Its resistance is bias-dependent.

Fig. (1.3)



Behavior of an MOS capacitor in the presence of a permanent inversion layer. C_{hf} is plotted versus V_G as a function of frequency. The usual hf behavior is only found for frequencies above the cut-off frequency of the external channel (70 MHz here). (After Nicollian, E.H. and Goetzberger A.

Fig. (1.4)

approximately the same technique as the one described in chapter-2 for the MOS transistor.

On the other hand, S.R.Hofstein and G.Warfield [5] have used a transmission-line model to analyze the lateral transfer of inversion charges which were supplied by the inverted regions outside the gate area. E.H.Nicollian and A.Goetzberger [6] have also used a transmission-line model, for the same purpose; their solution for the circular gate structure was in the form of Bessel functions.

In these two papers [5,6], they suggested a model like that outlined in Fig.(1.3).

In this model three components can be distinguished:-

1- The intrinsic MOS capacitor: which can be represented by the equivalent circuit commonly used , i.e. made up of oxide capacitance, of the space charge capacitance and of the capacitance C_{it} due to interface states.

2- The permanent inversion layer: Its electrons are free to move. The permanent inversion layer reacts in a double way to electric fields: in a direction parallel to the interface it behaves like a sheet resistance and in direction perpendicular to the interface, the inversion layer is capacitively coupled to the majority carriers of the semiconductor. The permanent inversion layer is therefore represented by a distributed resistance-capacitance network. It can be viewed as a transmission-line with low-pass filter characteristics.

3- The surface coupling resistance: it connects the MOS capacitor to the external channel and its value is bias dependent.

Fig.(1.4) shows the C(V) curves of this structure, the accumulation and depletion branches of the C(V) curves behave quite normally, because in these bias regimes the external inversion channel is disconnected from the MOS capacitor and exerts no influence. In inversion however, the channel is closely connected to the MOS capacitor and the rise of the high frequency capacitance is a direct consequence of this coupling. The input admittance of the channel shunts the space charge capacitance of the intrinsic MOS capacitor [4]. In what proportion the total A.C. current divides itself between the space charge (depletion) capacitance and the external channel depends on the frequency of the test signal. The channel current first spreads laterally before being led away through the capacitive leakage. The size of the area through which most of the channel current flows, is a measure of the effective shunt capacitance. It increases when the frequency decreases as the channel behaves like a low pass filter network.

Fig.(1.2) shows a representation of how this AC current flows. It is interesting that the C(V) curves in Fig.(1.3) is similar to that of the MOS transistor when its source, drain and substrate are tied together and grounded.

The above transmission-line models for the MOS capacitor with a surrounding extrinsic inversion layer, initiated the thought of similar transmission-line models to be applied for the MOS transistor, (which have a rectangular structure) to study its behavior. These models are presented in the next section.