DESIGN GUIDELINES FOR THE IMPLEMENTATION OF EMBEDDED NETWORK ON CHIP (NOC) IN FPGAS

By

Noha Gamal Mohamed

A Thesis Submitted to the
Faculty of Engineering at Cairo University
in Partial Fulfillment of the
Requirements for the Degree of
MASTER OF SCIENCE
in
Electronics and Communications Engineering

FACULTY OF ENGINEERING, CAIRO UNIVERSITY
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Under the Supervision of

Prof. Dr. Hossam A. H. Fahmy

Professor

Electronics and Communications
Engineering Department
Faculty of Engineering, Cairo University

Dr. Hassan Mostafa

Assistant Professor

Electronics and Communications
Engineering Department
Faculty of Engineering, Cairo University

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Approved by the
Examining Committee

_____
Prof. Dr. Hossam A. H. Fahmy, Thesis Main Advisor

_____
Prof. Dr. Amin Nassar, Internal Examiner

_____
Prof. Dr. Mohab Anis, External Examiner
(Electronics and Communications Engineering, The American University in Cairo)

FACULTY OF ENGINEERING, CAIRO UNIVERSITY
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Engineer's Name: Noha Gamal Mohamed
Date of Birth: 21/01/1987
Nationality: Egyptian
E-mail: noha_gamal@mentor.com
Phone: +20 1003826997
Address: Electronics and Communications Engineering Department, Cairo University, Giza 12613, Egypt

Registration Date: 01/10/2011
Awarding Date: --/--/2017
Degree: Master of Science
Department: Electronics and Communications Engineering

Supervisors:
Prof. Dr. Hossam A. H. Fahmy
Dr. Hassan Mostafa

Examiners:
Prof. Dr. Hossam A. H. Fahmy (Thesis main advisor)
Prof. Dr. Amin Nassar (Internal examiner)
Porf. Dr. Mohab Anis (External examiner)
(Electronics and Communications Engineering, The American University in Cairo)

Title of Thesis:

Design Guidelines for the Implementation of Embedded Network on Chip (NoC) for FPGAs

Key Words:
Network on Chip; Fields Programmable Gate Array

Summary:

In this thesis, a literature survey of existing Networks-on-Chips is presented, then a comparative review between the NoCs with available source code from area and speed respective is provided. Efficiency gaps between hard and soft implementations using FPGA-embedded NoC have been analyzed and designs recommendations have been proposed. Finally two soft implantations are introduced to attempt the maximum reduction of either the delay gap or the power gap between soft and hard implementations.

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Nomenclature

ASIC	Application Specific Integrated Circuits
ASSP	Application Specific Standard Products
BRAM	Block RAM
BSV	Bluespec System Verilog
CLB	Configurable Logic Blocks
DOR	Dimension Ordered Routing
DRAM	Distributed RAM
DSP	Digital Signal Processing
FF	Flip Flop
FPGA	Field Programmable Gate Arrays
FPSoC	Fields Programmable Systems on Chip
HoL	Head of Line
IP	Intellectual Property
LUT	Look Up Table
NCD	Native Circuit Description
NI	Network Interface
NoC	Network on Chip
NRE	Non Recurring Engineering
PAR	Place and Route
PCF	Physical Constraints File
PDR	Partial Dynamic Reconfiguration
QoS	Quality of Service
RLOC	Relative Location Constraints
SAMQ	Statically Allocated Multi Queue
SoC	Systems on Chip
VC	Virtual Channel
WSF	West Side First

Abstract

The continuous increases in the complexity of semiconductor manufacturing from technical and economical perspectives become a main concern to the applications dominated by application-specific integrated circuits (ASICs) and application-specific standard products (ASSPs). In contradiction to the increasing cost, complexity and risks of the dependancy on ASIC implementation process, field-programmable gate arrays (FPGAs) costs and time-to-market are looking very promising. FPGA industry has been developed gradually to minimize the risk and time consumed in the development of new products and increase the life time of the product in the marketing due to its flexibility of being reconfigurable, which consequently decrease the threat of being obsolete caused by introducing into the market same products with new generations.

Earlier FPGAs were only useful for applications with low densities or for ASIC prototyping. Nowadays, FPGAs serve as Fields Programmable Systems on Chip (FPSoC) and are widely used to implement computationally intensive world applications.

One of the major challenges of the FPGAs is the limited routing and logic resources. Moving towards newer FPGA technologies, the consumed power in routing becomes more than the power consumed in logic. Moreover; as the number of components in FPSoCs increases, traditional bus based and point-to-point interconnect schemes become bottlenecks in satisfying systems requirements. Consequently, embedding an efficient NoCs within FPGAs becomes essential to implement SoCs designs.

We first review several NoC designs based on their contributions, architectures, implementations and future works. We also make our comparison between three of these routes to analyze the effect of varying NoC parameters on the operating frequency and area utilization to help choosing the appropriate NoC based on system requirements. Then we use FPGA-embedded NoC design and compare implementing its components on soft and hard implementations to analyze the efficiency gap in area, frequency and power between the two design flows (i.e., FPGA flow and ASIC flow) and get the design constraints in this space. Finally we propose two different configurations in soft implementation using the FPGA-embedded NoC, one configuration attempts reducing the delay gap as much as possible between hard and soft implementations and the second configuration relaxes the delay gap constraint for a significant power reduction.

Chapter 1 : Introduction

1.1. Motivation

Implementation medium is one the important factors impacting the Systems on Chips (SoCs) configurations and their interconnect mechanisms in terms of performance and cost. Recently, FPGAs are gradually replacing ASICs because of FPGAs strength points of being easy to be upgraded, having short time to market and low development costs, providing immediate results and fast design cycles which make them the appropriate candidates for research proposes and removing the burdens of IC fabrication involvement and manufacturing operations. Although there are always continuous enhancements in FPGAs to reduce their weakness points and increase their capabilities, they always consume more power and area; operate on lower frequencies than ASIC and have limited and fixed resources. These are challenges for FPGAs to satisfy some systems' requirements.

Basic elements in FPGA are the programmable logic element for performing logic calculations and interconnect for data transfer. Recent FPGAs contain hardware and software blocks, such as memories, processors and Digital Signal Processing (DSP) blocks.

As systems complexity increases, bus-based interconnections become a bottleneck since they are unable to meet systems requirements. ARM's AMBA [1] bus and IBM's CoreConnect [2] are shared buses; they allow reusing intellectual property (IP) and support working with modular designs that have standard interfaces. But they are not suitable for large systems because of the performance degradation. Consequently FPGA vendors introduced an enhanced architecture that provides original standard shared bus besides direct module to module communication. This architecture is called hybrid bus/direct interconnection. These enhancements came with the cost of reducing systems modularity and adding more effort for customizing hardware designs for the module to module connection which complicates design process. Bus segments architecture was introduced to rebalance the load of the bus. It is suitable for modules communicating on the same segment with no congestion to the rest of the bus. However this complicates the design process and reduces systems scalability and flexibility [3].

Network on Chip (NoC) is the candidate as a subsystem for the communication between IP cores in a system on chip to overcome all previous problems. Strength points of NoCs are scalability and flexibility because of the optimization and the independent implementations between layers. They can work in both synchronous and asynchronous clock domains, support different topologies. They provide interface interoperability using simplified customization per application. They also enable interface with high speed inputs/outputs like PCI-Express.

Embedded hardware, software blocks and customizable logic blocks within the FPGA architecture make it the typical choice for NoCs designs. Implementing NoC with low area overhead in FPGAs and choosing the appropriate set of NoC parameters are necessary because of the limited routing and logic resources.

NoCs on FPGAs enable implementing one of the most promising features which is partial dynamic reconfiguration (PDR). It is the ability to change the logic of one of FPGA blocks without interrupting the other blocks while they are running.

1.2. Contribution

This dissertation of this work includes the following contributions:

- Provide a review on different NoC designs, their architectures, simulation and test results.
- Compare between three open-source NoCs to analyze the behavior of the NoC with varying NoCs parameters and to help selecting the NoC design that would match to system requirements using soft implementation.
- Choose FPGA-embedded NoC and measure area allocation, maximum operating frequency and power consumption on the sub-module level of the router in both hard and soft implementations and compare between the results of soft and hard implementations. Then provide design suggestions whether each module in the NoC is more suitable to be harden or to be reconfigurable. And investigate whether the NoC would give better results in soft implementations if it is designed to target FPGA than NoCs designed for ASIC or not.
- Introduce two different configurations for the soft implementation. First configuration attempts reducing the delay gap between soft and hard implementations as much as possible. The second configuration results in a significant reduction of consumed power with a small increase in area and delay gaps. Results are measured on the network level.

1.3. Organization of the Thesis

The remainder of this thesis is organized as follows. Chapter 2 provides a detailed survey of the most recent NoCs with their architecture and simulation results, then makes a unified comparison between NoCs with available open source code . Chapter 3 uses FPGA-embedded NoC and compares its behavior under soft and hard implementations on sub-module level, then gives design recommendation for each module for best implementation. Chapter 4 introduces two soft implementations for the FPGA-embedded NoC and studies the two configurations behavior on network level to give design suggestions which configuration to use according to the target applications. Then the thesis conclusion and future work are revealed in “Discussion and Conclusion” section.

Finally, Appendix A shows the steps required for accurate estimation of power and area in soft implementation. While, Appendix B gives a detailed description for the created scripts used for automating the measurement of the efficiency parameters.

Chapter 2 : Literature Survey of Existing Networks-on-Chips

2.1. Introduction

In this chapter, we give an overview of FPGA and ASIC advantages and disadvantages, and then highlight the importance of NoCs especially for FPGA. Then we explore previous works of different NoCs designs that represent the core of most NoCs designs in the literature recently. We show their contributions, architectures, implementation, test results and future works. Finally we make our comparison between three NoCs across different values of the NoC parameters to give design recommendation to help choosing the appropriate NoC according to system requirements.

2.2. FPGA versus ASIC

FPGAs and ASICs address different market requirements. In the past, FPGA used to be dominant for only prototyping and applications with low complexity, speed and volume. Currently FPGAs replace ASICs for low and medium applications due to the major enhancements introduced to FPGA's operating frequency, chip density and fabrication cost. Although ASICs have better performance characteristics (speed, area and power), FPGAs keep pushing ASICs from market mainly because of their flexibility and quick time-to-market values.

2.2.1. Unit Costs

Although ASIC has higher R&D design costs, in high volume applications, it has lower costs of manufacturing than FPGA as shown in Figure 2-1.

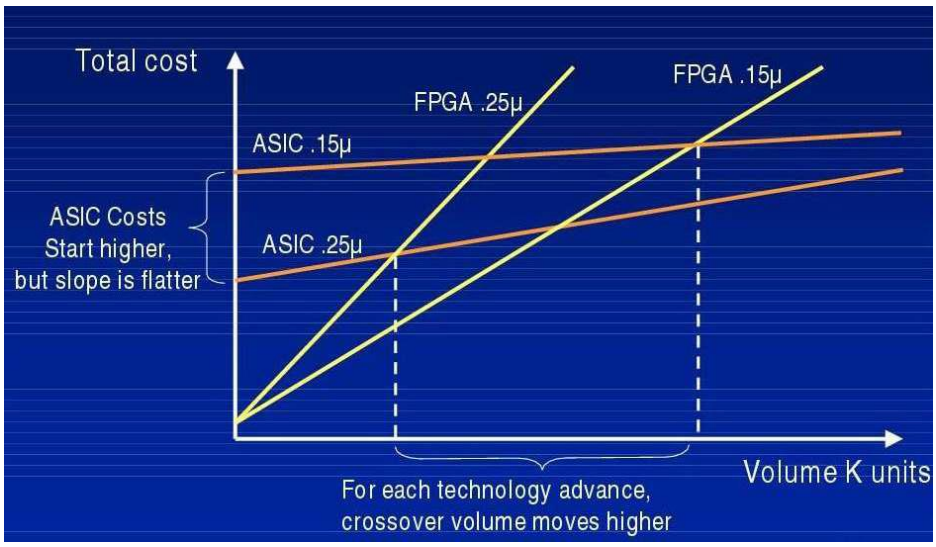

Figure 2-1: FPGA vs. ASIC Cost