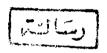
Ain Shams University Faculty of Engineering

NEW DYNAMIC TECHNIQUES FOR MAPPING GENERAL PARALLEL NESTED LOOPS ON MULTIPROCESSOR SYSTEMS

By

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A Thesis



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To my father and mother whose love, encouragement, patience and faith made this all possible.



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STATEMENT

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The work included in this thesis was carried out by the author in the Departement of Computer and Systems Engineering, Ain Shams University, and in the Departement of Computers and Systems in the Electronics Research Institute (National Research Center).

This thesis had been published in two papers, but no Part of this thesis has been submitted for a degree or qualification at any other University or Institution.

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NEW DYNAMIC TECHNIQUES FOR MAPPING GENERAL PARALLEL NESTED LOOPS ON MULTIPROCESSOR SYSTEMS

Abstract -- As device technology approaches physical limitations, parallel processor systems offers a promising and powerful alternative for high performance computing. In principle parallelism offers performance that can increase without bounds and depends only on the applications in hand. In reality parallelism have its limitations, such limitations is due to two main obstacles.

The first obstacle is that the technology is still unable to support the realization of parallel machine with large number of general purpose processors. The second and the greater obstacle appears which is our inability to efficiently utilize such massively parallel systems. Problems such as specifying parallelism, mapping or scheduling parallel programs on a given architecture, synchronizing the execution of a parallel programs, memory management in parallel processing environment, and compiling for parallel machines remain areas for new research.

In numerical or scientific programs, nested loops are the most time consuming parts in serial processing but at the same time offer the most amount of parallelism from the sight of parallel distributed processing. Our concern in this thesis will be the schedules which instruct such nested parallel loops for the processors.

One of the most promising schedules which appears in this field is the "Two-Level Self-Scheduling" algorithm which divides the nested parallel loops scheduling process into two levels of scheduling. a) The high level scheduling; in which the loop instances are placed in a task pool and then chosen for execution, and b) the low level scheduling; in which the processors dispatches a single iterations from any task which requires processors to complete its iterations.

The main disadvantage in this algorithm is that the loop indexes shared variables (which requires semaphore locking and unlocking) had to be updated a number of times equal to the loop bound due to the mandatory private access to such indexes.

In this thesis we present the "Two-Level Guided Self-Scheduling" algorithm and the "High Gain Two-level Guided Self-Scheduling" algorithm , two new approaches for scheduling

arbitrarily nested parallel programs on shared memory multiprocessor systems.

The first proposed algorithm is a modification for the low level part of the "Two-Level Self-Scheduling " algorithm using the "Guided Self-Scheduling " technique, such that each processor instead of dispatching a single iteration each time according to the "Self-Scheduling " technique, it dispatches a number of iterations calculated according to the "Guided Self-Scheduling " technique. This reduces the number of updates of the tasks indexes from a value equal to the loop bound to a value equal to the number of processors. This causes this algorithm to become of more load balancing and of very low synchronization overhead.

The second proposed algorithm contains a farther enhancements to the "Two-Level Guided Self-Scheduling" algorithm to decrease its scheduling time and increase its time gain greatly over the "Two-Level Self-Scheduling" algorithm in the case of systems with large number of processors but with some restrictions in the algorithm applicability.

After presenting the proposed algorithms a real simulation environment based on a Local Area Network system (LAN) to simulate a time shared BUS tightly coupled multiprocessor machine.

In this simulation the LAN workstations is the analogy of the processors of the multiprocessor system (by making such workstation execute the scheduling algorithm) and the LAN server hard disk is the analogy of the shared memory of the system (by creating the task pool on this disk as a number of data files)

Based on this simulation environment a performance comparison is made between the "Two-Level Guided Self-Scheduling" algorithm and the "Two-Level Self-Scheduling" algorithm to show to what extent such algorithm is useful.

From the results obtained in such performance comparison are the Time versus Number of processors, the Multiprocessor system time utilization percentage versus the Loops bound and the Multiprocessor system time utilization percentage versus the Multiprocessor system time utilization percentage versus the Number of processor for both the "Two-Level Self-Scheduling" algorithm (T.L.S.S.) and the "Two-Level Guided Self-Scheduling" algorithm (T.L.G.S.S.) and the time gain percentage of the T.L.G.S.S. algorithm over the T.L.S.S. algorithm.

From these results it was clear that the "Two-Level Guided Self-Scheduling" algorithm increases the Multiprocessor system time utilization and decreases the time required to execute the same tasks over the "Two-Level Self-Scheduling" algorithm.

Also based on this simulation a performance comparison is done between the "High Gain Two-Level Self-Scheduling" algorithm (H.G.T.L.S.S.) and the "Two-Level Self-Scheduling" algorithm (T.L.S.S.) including the time gain percentage of the H.G.T.L.G.S.S. algorithm over the T.L.S.S. algorithm.

From this comparison it was clear that the H.G.T.L.G.S.S. algorithm gives a linear increase in the time gain percentage over the T.L.S.S. algorithm in the case of large number of processors in the contrary to the T.L.G.S.S. which gives a very small time gain percentage over the T.L.S.S. algorithm in this region.

Finally some notes about the future trends in scheduling parallel programs on distributed memory multiprocessing systems is included.

CHAPTER 1

Introduction