COMPUTER AIDED DESIGN
OF
MOS/LSI

A THESIS

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MASTER OF SCIENCE

BY

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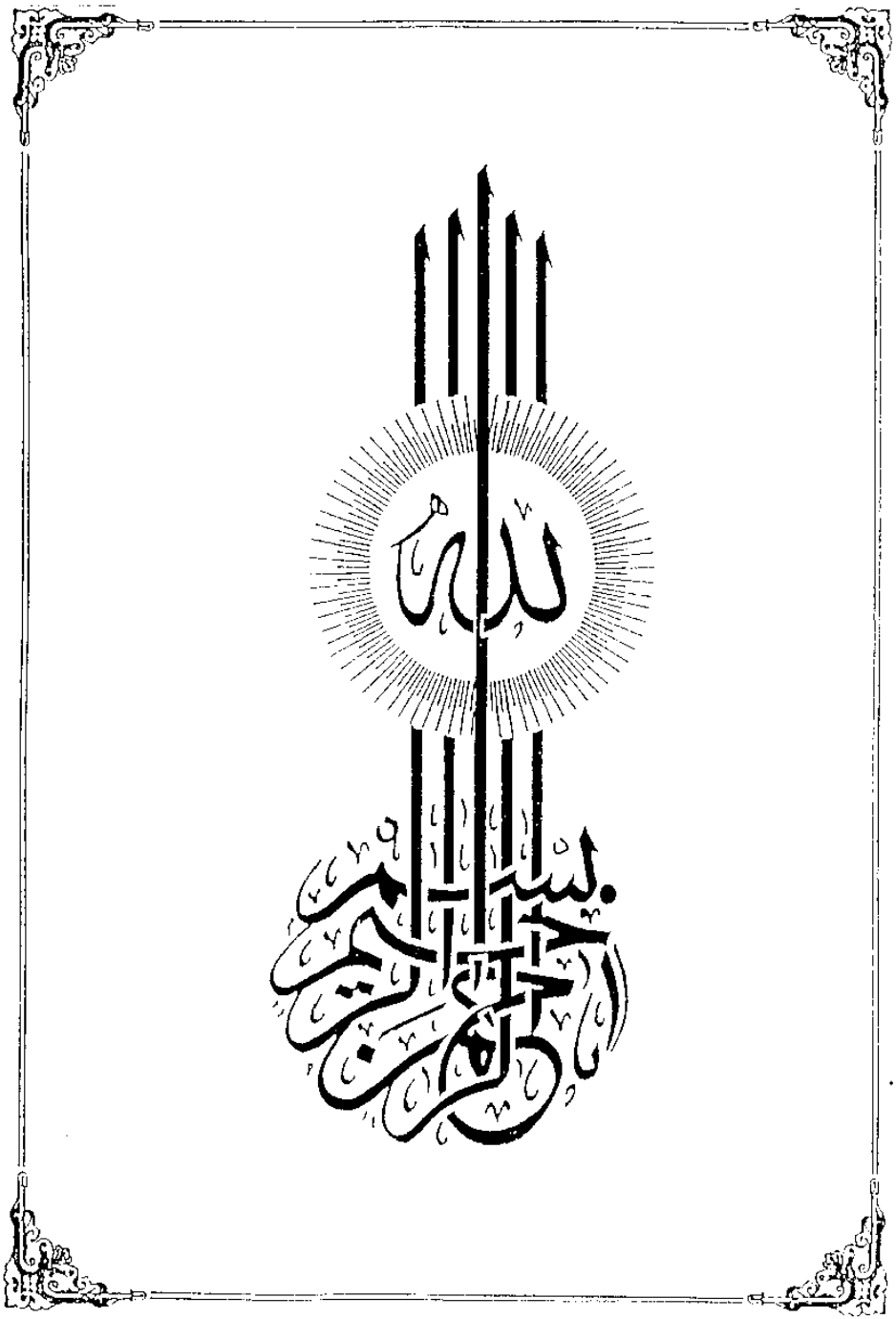

APPROVAL SHEET

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CONTENTS

SUMMARY

The aim of the present work is to develop a macro-modeling technique, which would describe an integrated digital gate as an entity rather than a group of separate devices. This approach is based on an analytical formulation of the input-output gate relationship. Hence this technique is advantageous in the design and analysis of large scale integrated circuits (LSI).

Chapter (1) deals with the studying of electronic structures based upon the metal-oxide semiconductor technique. Also the related physical and technological bases were reviewed and discussed. This was essential to establish the necessary background required for the research.

Chapter (2) deals with the development of a computer calculator circuit simulation technique to obtain the dc characteristics of MOS digital integrated circuits. The computations of these dc characteristics were derived in terms of the device physical parameters which are extracted from processing data. The computed results were found to be concident with measurements in the literatures.

In chapter (3), a macromodeling of the transient response was derived analytically for the MOS digital

gate. This was found to be more accurate, more generalized, and less complicated than the existing techniques. This macromodel was applied to an "FMGB-55" NOR gate, where the computed transient response was found to be in good agreement with published experimental results.

Chapter (4) contains the derivation of a macromodeling of transient response for the complementary metal-oxide semiconductor (CMOS) LSI. This is done for the CMOS digital gate. The computed results using this derived macromodel were compared with those using "SCEPTRE" computer program and with published experiment results were a good agreement is again found to be existing.

Chapter (5) explains a technique for the application of the already derived dc and transient macromodels on a complex logic circuit. A master-slave flip flop is chosen as an example to verify this technique.

Finally, the conclusions of the whole study is presented in chapter (6).

LIST OF SYMBOLS

C_B Substrate impurity concentration

C_{ou} The load capacitor

C_o Specific gate-oxide capacitance

dy Incremental distance along the channel

I_D Drain current

K_o Relative dielectric constant of oxide

K_s Relative dielectric constant of silicon

L Channel length

$L_{dep.}$ Reduction in channel length in saturation

N_A P-type impurity concentration

N_D N-type impurity concentration

Q_B Depletion charge at the onset of strong inversion per unit area

Q_I Inversion charge per unit area

$Q_p(y)$ Coefficient used in the MOST four-terminal model derivation

$$Q_p(y) = - \left[V_G - V_{FB} - 2\phi_f - V(y) \right] C_o - \left[2 K_s \epsilon_o q C_B \left| V(y) + 2\phi_f \right| \right]^{\frac{1}{2}}$$

Q_s	Total charge within the semiconductor per unit area
Q_{ss}	Positive charges at Si - Si O_2 interface
t_{ox}	Gate-oxide thickness
V_{BG}	Back-gate substrate voltage
V_D	Drain voltage
V_{FBn}	Flat band voltage for n-channel MOST
V_{FBp}	Flat band voltage for p-channel MOST
$V_{Dsat.}$	Drain saturation voltage
V_G	Gate voltage
V_{in}	Input voltage
V_o	Output voltage
V_{osn}	Output saturation voltage for n-channel MOST
V_{osp}	Output saturation voltage for p-channel MOST
V_{ox}	Voltage across the Si O_2 (gate oxide)
V_s	Source voltage
V_{To}	Turn-on voltage

$V(y)$ Potential along the channel

R_s Parasitic drain and source series resistance

X_o Thin-oxide thickness

X_d Depletion layer width

Z Channel width

β Ratio of driver and load MOST's current factors

$$\beta = \frac{\mu_D \ (Z/L)_D}{\mu_L \ (Z/L)_L}$$

$\mu_{eff.}$ Effective mobility in the inversion layer

ϕ_{fp} Fermi potential for p-type MOST

ϕ_{fn} Fermi potential for n-type MOST

ϕ_{ms} Work function difference between metal gate and semiconductor

ϕ_o Coefficient used in the I-V relationship

$$\phi_o = \frac{2 \ k_s \ \epsilon_o \ q \ C_B}{C_o^2}$$

ϕ_x Coefficient used in the I-V relationship

$$\phi_x = (\phi_o \ | 2 \ \phi_f |)^{\frac{1}{2}}$$

Φ_y Coefficient used in representing the saturation region

$$\Phi_y = \frac{\Phi_o}{2} + \Phi_x$$

CHAPTER (1)

PHYSICAL AND TECHNOLOGICAL CHARACTERISTICS OF METAL-OXIDE SEMICONDUCTOR TRANSISTOR (MOST)

(1-1) Introduction.

The MOST is the basic and unique cell used in MOS integrated circuits, which makes it possible to construct large scale integration (L SI). Thus in this chapter we are concerned with the physical and technological aspects of the MOST.

The analysis of MOST begins with the study of the semiconductor surface, this can be accomplished by studying the MOS (metal-oxide semiconductor) structure which is the basic inherent part of MOST.

MOS structure is studied first in section (1-2) in its ideal case, where the principale of operation is presented. The analysis of turn-on voltage in the ideal case is accomplished in section (1-3). Section (1-4) deals with the actual MOS structure contains many effects which make it not ideal. The back gate bias technique and its effect on the threshold voltage will be discussed in section (1-5), while in section (1-6) all the MOST equations will be derived. Section (1-7) will contains all the

factors which effect the MOST operation. At the end of the chapter, a brief note will be given on the different techniques used in MOST fabrication which will be included in section (1-8).

(1-2) Ideal MOS structure [1, 2, 3].

Consider a p-channel MOST structure as shown in Fig. (1-1-a) where the work function between metal gate and silicon $\Phi_{MS} = 0$, charge in the gate oxide $Q_{ox} = 0$, and charge at the silicon-silicon dioxide interface $Q_{ss} = 0$. The energy - level structure for the device in the n-region under the gate oxide, with source, substrate, gate and drain grounded is shown in Fig. (1-1-b). The horizontal structure of the energy levels is referred to as the flat - band condition. It is to be noted that the energy - level diagram is now two dimentional, with distance into silicon represented in the horizontal direction, and electron energy represented along the vertical direction. The on-state of the MOST is achieved by applying a gate voltage V_G of proper polarity between the metal gate and the silicon substrate. An applied negative - gate voltage V_G sets up on electric field which in turn bends the energy bands in the bulk silicon to the extent that E_i crosses E_f and the surface region becomes p-type