Ain Shams University
Faculty of Engineering

" Digital MOS Multilevel Circuits "

By
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A Thesis

ıbmitted in partial fulfilment for the requirments of the degree of M.Sc in Electrical Engineering

upervised By :
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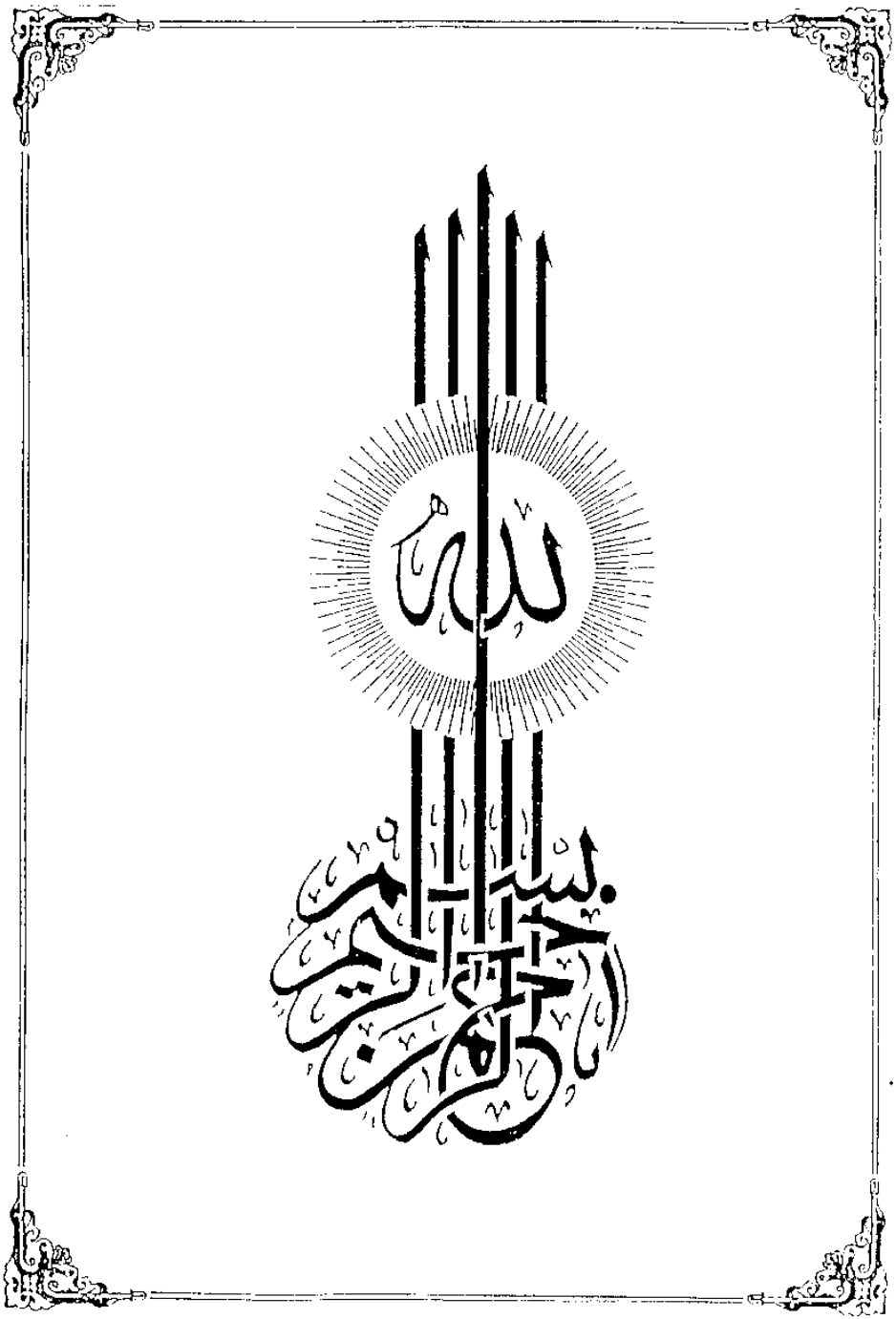

Statement

This dissertation is submitted to Ain Shams University for the degree of M.Sc in Electrical Engineering.

The work included in this thesis was carried out by the author in the department of Electronics and Computer Engineering, Ain Shams University, from october 1986 to august 1989.

No part of this thesis has been submitted for a degree or a qualification at any other university or institution.

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As the VLSI technology grows rapidly, the problem of interconnections that characterize the VLSI circuits becomes more severe. One solution is the use a three dimensional integrated circuits, vertical integration. Another approach is to increase the quantity of information carried by each conducting line on the chip, namely, multivalued logic signaling.

In this thesis we are taking, in the first place, the trends towards multivalued logic signaling. We are concerned with the electronics of the MVL circuits. In other words, the design methodologies and the corresponding technology that will match for a certain design are the main objectives of this work.

In chapter.1, we have introduced a general overview of MVL signaling and the representation schemes for its functions. Classification of MVL modes in terms of voltage, current, and charge are also introduced. The different areas of Multivalued logic applications are discussed.

In chapter.2, The modeling of the MOS parameters due to scaling down effects will be discussed. For instance, the odeling of the threshold voltage will help in finding the circuit noise margin and speed. Hence, this thesis introduces a scaling down analysis for the MVL circuits. We are using the circuits analysis program "IS-SPICE" for circuits simulation. At the end of each chapter, we can find a list of the "input decks" referenced to that chapter.

In chapter.3, the basic building blocks of MVL circuits have been proposed, in voltage mode and current mode. Circuits simulation and practical measurements have been made to identify the circuits operation. From this analysis we have deduced the aximum number of logical levels that can be used in the proposed MVL circuits.

In chapter.4, the T-Gate is used as a basic building block in the design of MVL functions. The different applications discussed in this chapter are :

1) Implementing some combinational and sequential MVL functions, using twelve Ternary T-Gate implemented in the lab.

2) Design and simulation of MVL encoder, which simulate the error correcting code of Quaternary message.

3) Designing a circuit that detect the stored level in Quaternary ROM, where each cell stores a single quat (equivalent to 2 bits).

A final conclusion was made about the potential applications of MVL signaling . To clarify the advantages and disadvatages of MVL, a comparison is made between Binary and MV signaling.

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Chapter (1)

Multiple-Valued Logic

1.1 Introduction :

The multiple-valued logic has been the object of much research over the last twenty years. Since 1971 , there has been an annual symposium devoted exclusively to the multiple-valued logic. Much of the older work was of a purely theoretical nature concerned with the functional completeness of operators , functional minimization , and those problems related to the switching theory and logical design .

The main direction for the work in multiple-valued logic is the urgent attempts to reduce interconnection complexity and reduce chip area on VLSI circuits . With the trends towards further miniaturization , VLSI chips containing random logic will approach various fundamental limits , i.e , geometrical , thermal , and electrical limitations [24] . The scaling down of the integrated circuit elements will allow the production of elements with linear dimensions of less than 0.1 μm . In this case, scaled transistor structure will be limited essentially by its physical limitations which are not inherently affected by miniaturization, i.e, depletion layer . This limitation is expressed in the Moore and Noyce law illustrated in figure (1.1), [3] . In this figure, the number of devices per unit area increases exponentially . This exponential increase will not be limited by physical considerations before 1995 , and after that , further increase in

packing density or functions might depend on more relevant technologies and techniques , i.e , three dimensional vertical integration [32] and Multiple-Valued Logic .

This chapter will be devoted to the multiple-valued algebra and the directions for the design of multiple-valued circuits . Finally , the application areas of MVL will be displayed.

1.2 Multiple-Valued Algebra

Binary integrated circuits implement the basic operators of boolean algebra . In case of multi-valued signals, the circuit implement post algebra . A multivalued signal of radix M occurs as an ordered set of values of a signal variable , perhaps voltage ,current , or charge . The labelling of a multivalued signal variable is an extention of the binary case , namely, 1,2,3,.....,M-2,M-1 . A second convention called the balanced labelling is also used with odd radices and signed numbers . It requires an odd radix R = 2m + 1 , and values (-m), (-m+1), (-m+2),..,-1,0,1,..,m-1,m .

The early work in Multiple-Valued Logic was mainly directed to establish an ideal set of logic elements or operators , a complete set which combines between the convenience of analysis and implementation . It was apparent that such requirements will be highly dependent on the technology advance . As a result , a large number of these functions has been proposed . Some of this operators are easy to implement in one technology and difficult in another. Table (1.1) provides a summary of many multiple-valued operators (functions) including a positional

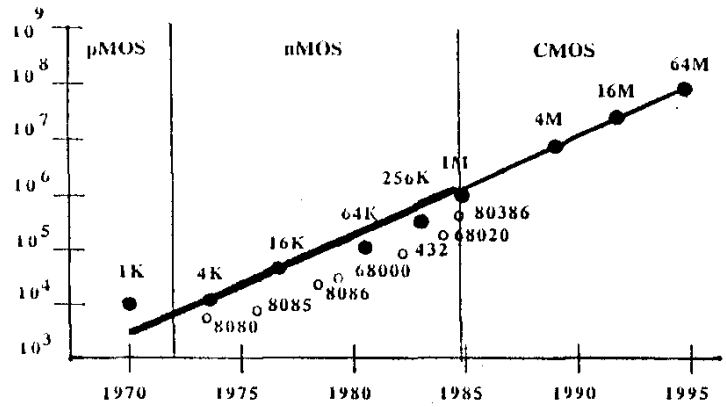

Figure 1.1 Moore and Noyce law.

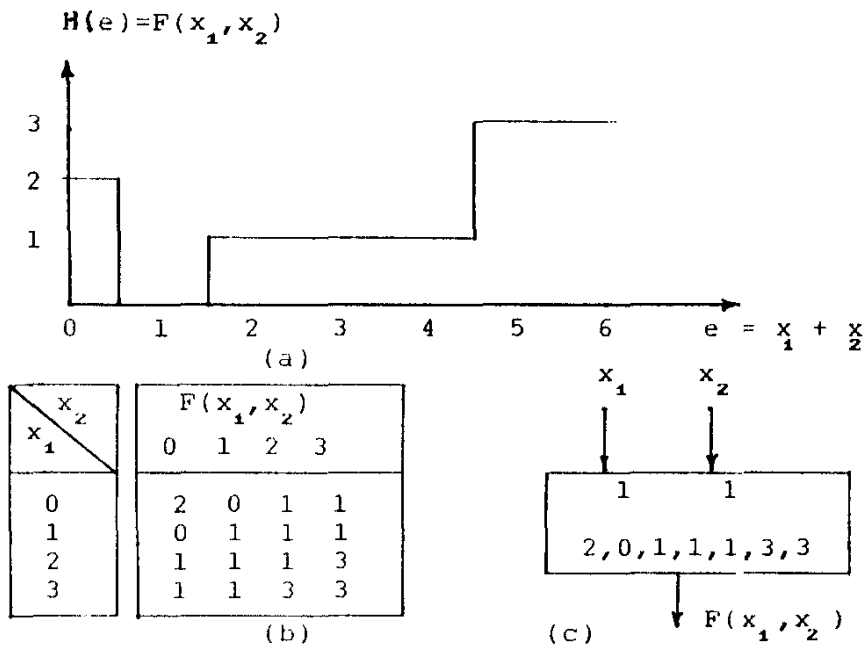

Figure 1.2 A three threshold two-input MT(4) gate with unity weighting.(a) Truth table. (b) Transfere function.(c) Symbol.

TABLE 1.1
Multivalued Function Notation and Discribtion

NO.	Commen Name	Symbolic Notation: Primary, Secondary	Symbolic Notation: Positional Base 4 example a=1, b=2, y=x	Value, Condition
1	Restoring, Identity	x	<0123>	x standerdized
2	(Diametrical) Inverse or Complement	$\tilde{x}$	<3210>	(R-1) - x
3	Maximum	max(xy), x+y or $x \vee y$	<3223>	x if x ≥ y else y
4	Minimum	min(xy), x.y or $x \wedge y$	<0110>	x if x ≤ y else y
5	Successor	$\vec{x}$, suc(x)	<1230>	(x+1)mod R
6	Cycle, (Clockwise Cycle)	$\vec{x}^b$, $\vec{x}^1 = \vec{x}$	<2301>	(x+b)mod R
7	Counter Cycle	$\overleftarrow{x}^b$, $\overleftarrow{x}^1 = \overleftarrow{x}$	<2301>	(x-b)mod R
8	Literal function	${}^a x^b$, x(a,b)	<0330>	(R-1)if a≤x≤b, else 0
9	DElta Literal function	${}^a x$, $J_a(x)$	<0300>	(R-1) if x=a, else 0
10	Closed Interval	$[a\ x\ b]$	<0110>	1 if a≤x≤b, else 0
11	Open Interval	$]a\ b[$ x	<0000>	1 if a<x<b, else 0
12	Delta Interval	$[a\ x\ a]$	<0100>	1 if x=a, else 0
13	Threshold Literal	$U_a(x)$	<1100>	1 if x≥a, else 0
14	Step Literal	$D_a(x)$	<1100>	1 if x≤a, else 0
15	Truncated Difference	x ⊟ a	<0012)	x-a if x≥a, else 0
16	Truncated Sum (Limited Sum)	x ⊞ a	<1233>	x+a if <R-1, else R-1
17	T-GATE, Multiplex	T(x,y,q)	<0123) <3210)	x if q=0, y if q=1
18	Multithreshold MT(R)	$[H_1 \ldots H_m]$ $(K_1 \ldots K_n)$	<pqrs)	Use a threshold sum to look up a table of values

notated example . In the table , one can identify the relationship between the post operators and its circuit implementation . Moreover , we can also identify the type of technology that will copy conveniently with the desired function. For example , the truncated difference and the truncated sum are denoted $x \boxminus a$ and $x \boxplus a$, respectively , may be implemented easily by using Charge Coupled Devices (CCDs) technology . On the other hand , the CCDs technology will not be adequately used in implementing other functions such as the MAX. and MIN. operators. In this table , one can also note the relationship between the different operators . For example , the interval and the lateral gates are related as follows :

$$x^{a\ b} = (m - 1)\ x^{[a\ b]}$$

and

$$x^{[a\ b]} = MIN(1\ ,\ x^{a\ b})$$

Where the position of (m - 1) implies multiplication .

Two of the logic functions in the table deserve more attention . They constitute logically complete operators, where any multiple-valued function could be implemented using one of these operators , namely, the T-gate and the multithreshold radix r gate , MT(r) . The T-gate is functioning as a multiplexer controlled by a multivalued signal variable.

In the MT(r) shown in figure (1.2) , each input is weighted and summed and the sum compared against a multivalued reference . For each value of the weighted sum, a particular output is

defined. Hence, the MT(r) and the T-gate do not correspond to post algebra , they are a threshold functions , which are a well known subset of binary functions . It should be noted that ease of algebric manipulation is no longer of great interest , as depicted by the trends toward the tables and pattern-oriented schemes .

1.3. Characterization of MVL Circuits by Physical Variables

The design of multi-valued circuits considers one or more of three variables, namely, charge, current, and voltage.

1.3.a Charge mode

The basic idea of the charge mode circuits is the storage of charge in a well with a certain capacity . The signal charge is introduced by means of " fill and spill " . The capacity of the well is controlled by the following formula :

$$Q_{max} = C(V_1 - V_2).A$$

Where A is the storage gate area , V_1 its potential , V_2 the potential of the adjacent electrode , and C is a capacitive constant . In the CCDs, the voltage is internally used to couple the input and the output variables. Figure (1.3) shows the principle of charge transefere with the clocking waveforms and the output coupling circuitry .

The charge coupled devices (CCDs) technology uses the charge for information transfere in an clocked sequential environment. This technique will allow continuous signal processing with the availability of building memory and logic. Since CCDs are used in analog and binary environment, it can be used in implementing MVL

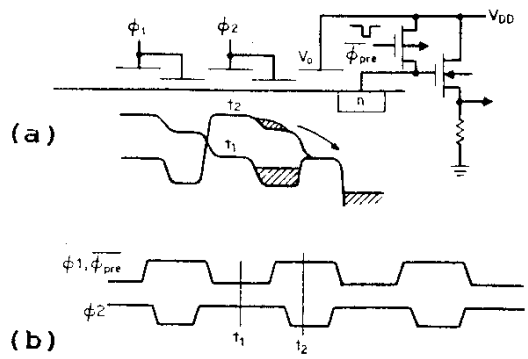

Figure 1.3 A CCD output circuitry. (a) Device cross section with surface potential profile. (b) clocking waveforms.

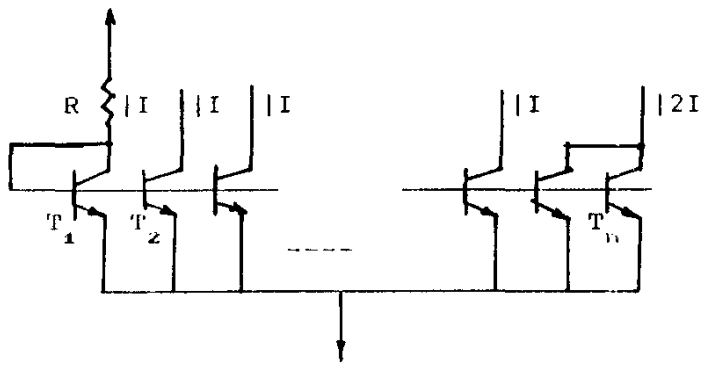

Figure 1.4 A current mirror (current sink)

circuits, namely, charge mode MV circuits.

1.3.b Current mode

The fundamental element for MV current mode logic systems is the current source , usually having a multiplicity of outputs. In the real implementation , such current source uses a current mirror as shown in figure (1.4). The current I is forced to flow through T_1 , a replica of this current is mirrored to T_2-T_n . Multiple of the basic current is also available at the output branches . In this figure , the collectors of T_n and T_{n-1} are connected together to provide a current 2I .

The ECL technology is also used in the design of current mode MVL functions, with the advantage of high speed operation. Figure (1.5) shows an example of a restorer, or identity gate with ECL technology, where each difference amplifier pair act as a binary comparator. Each comparator pair have its own reference threshold. The input variable is current which is passing through T_1 and mirrored to T_2. The voltage drop across R wil be compared with the different thresholds, which are equally-spaced and ground-referenced voltages, V_{T1}- V_{T4} . The transistor T_{11} is passing a unit step current I_o, which is mirrored through T_{12}- T_{15}. If the voltage at the point S is less than the threshold of a certain comparator, this comparator will switch a current I_o to the output, increasing the output current by one unit.

It should be noted that the addition of the resistor r in the branch of T_1 will make it possible to use an input voltage