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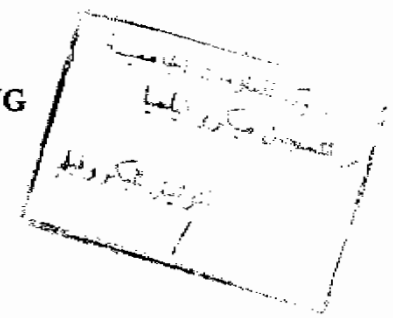

رسالة

ANALOG VLSI NEURAL NETWORKS

By

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B.Sc. in Electrical Engineering

A Thesis
Submitted In Partial Fulfillment For
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Supervised by

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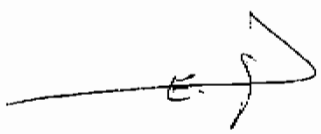
1.	Prof. Dr. Elsayed M. Saad, Helwan University.	
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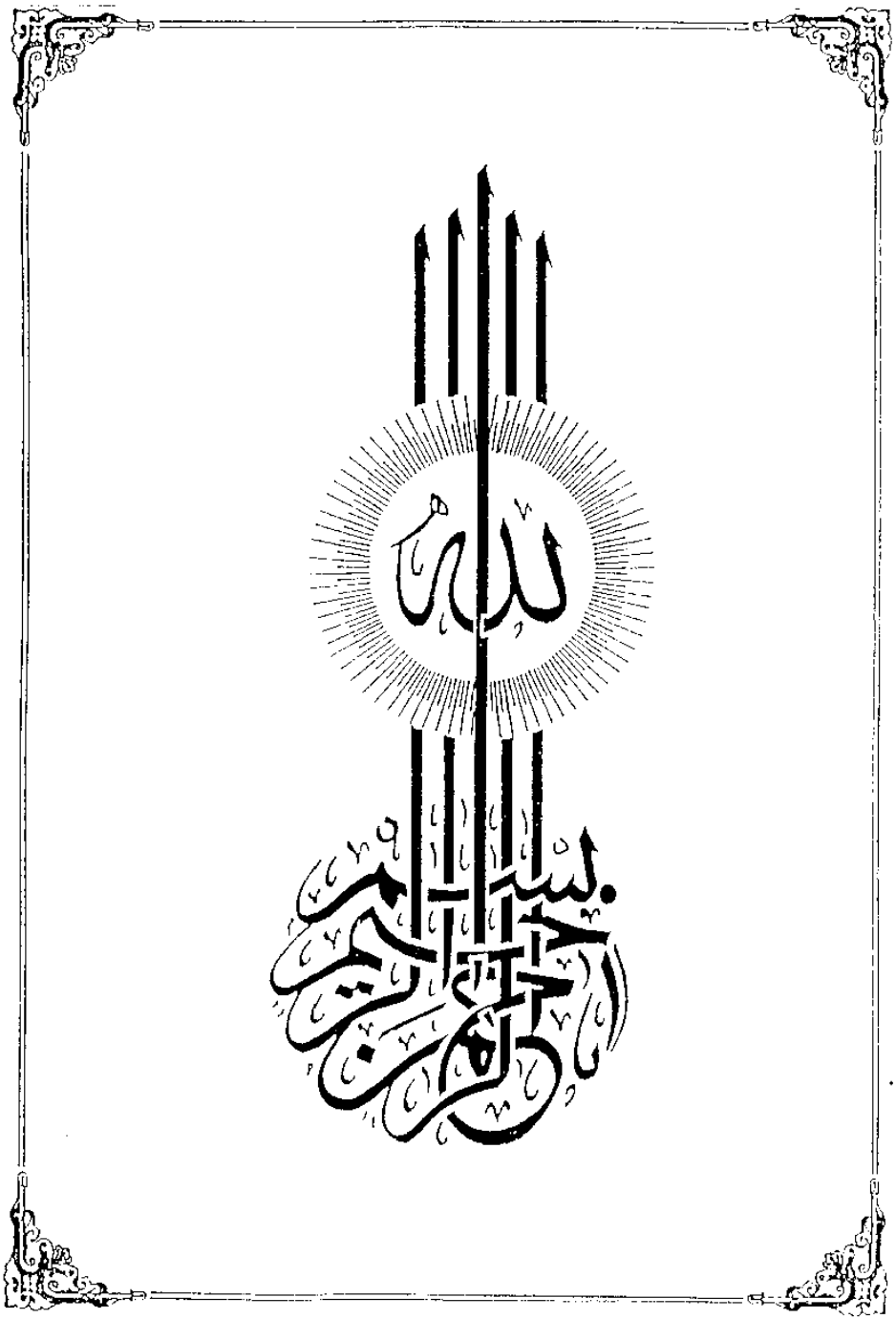

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STATEMENT

This dissertation is submitted to Ain Shams University for the M.Sc. degree in Electrical Engineering.

The work included in this thesis was carried out by the author in the Electronics and Communication Engineering Department, Ain Shams University, from December 1992 to September 1994.

No part of this thesis has been submitted for a degree or a qualification at any other university or institution.

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To the soul of my father

To my mother and my wife

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ABSTRACT

Some of the famous types of Artificial Neural Networks are discussed with special stress on the electronic implementation of their basic building blocks. An engineering oriented network, the neural-based A/D converter, is chosen as an example and studied thoroughly covering all aspects: theory, modeling, VLSI design and implementation with special emphasis on some state-of-the-art design techniques, namely the Analog Behavioral Modeling and the Automatic Model Generation.

SUMMARY

Chapter 1, Introduction

In this chapter a brief explanation is given for the meaning of *Analog VLSI Neural Networks*, their characteristics and main categories. A brief historical background is given and it is explained why the *analog* and *VLSI* techniques are used.

Chapter 2, Artificial Neural Networks

In this chapter Artificial Neural Networks (ANNs) are explained, elucidating their biological origin and explaining their main building blocks; neurons, synapses,... Some of the famous types and training algorithms are discussed. Namely the perceptrons, the backpropagation networks and Hopfield networks.

Chapter 3, CMOS VLSI ANN Building Blocks

A detailed discussion for two circuits is given, which are the differential amplifier and the comparator. These circuits represent the main building block of nearly all ANNs. Their behavior is studied in the strong inversion region for being the region of interest for our chosen ANN application. Design techniques for those circuits are thoroughly covered.

Chapter 4, Neural-Based A/D Converter

An engineering oriented ANN is chosen which is the Hopfield Neural-Based A/D Converter. We start with a complete theoretical background, then ideal and non-ideal modeling are performed using FAS and HDL-A languages supported by the ELDO simulator. Both types of modeling enabled us to fully understand and characterize the circuit, with many of the side effects and parasitics detected and understood. Thus making the design and implementation phases less troublesome.

The network is electronically designed and implemented, using full-custom methodology to the transistor level with all design details fully discussed. Simulation is carried out for the overall network, as well as for the components building up the network. All the obtained results are fully explained. The work was performed on a DEC station 5000/125 using the ELDO simulator.

Eventually, the ***conclusion*** is drawn.

In ***Appendix A***, a part of the CIF file describing the layout details of the neural A/D converter is given.

Appendix B shows the most important parts of the programs and ELDO files used in our modeling and simulation processes.

Finally, in ***Appendix C*** we show the submission forms needed by the silicon foundry for the chip fabrication.

LIST OF SYMBOLS

A	:	Area.
A_v	:	Voltage gain.
A_{vc}	:	Common-mode voltage gain.
A_{vdd}	:	Differential-input differential-output voltage gain.
A_{vds}	:	Differential -input single-ended output voltage gain.
β	:	$\beta = K'W/L$.
γ	:	Bulk threshold parameter.
λ	:	Channel length modulation parameter.
$C_{c(out)}$	:	Capactiance between output of comparators and ground.
C_d	:	Diffusion capacitance.
C_G	:	Gate capacitance.
C_L	:	Load capacitance.
C_{md}	:	Metal to diffusion routing capacitance per unit area.
C_{mf}	:	Metal to substrate (field) routing capacitance per unit area.
C_{mp}	:	Metal to polysilicon routing capacitance per unit area.
C_{ox}	:	Gate capacitance per unit area.
C_{pf}	:	Polysilicon to substrate (field) routing capacitance per unit area.
C_{pr}	:	Capactiance between polysilicon resistors and ground.
$C_{s(out)}$	:	Capactiance between output of switches and ground.
E	:	Energy function of a Hopfield ANN.
ε_0	:	Permittivity of free space.
ε_r	:	Relative permittivity (Dielectric constant).
ϕ	:	Strong inversion surface potential.
GAP_i	:	Difference between the lower and upper limits of analog input voltage decided by the ith amplifier.
g_m	:	Transconductance.

g_{md}	:	Differential output transconductance.
I_i	:	Input current to the ith amplifier.
I_{OD}	:	Differential output current.
I_{SS}	:	Sum of the two branch currents in the differential amplifier ($I_{SS}=I_{D1}+I_{D2}$).
K'	:	Tranconductance parameter, ($K' = \mu\ C_{ox}$).
L	:	MOS channel length.
μ_n	:	Electron mobility.
μ_p	:	Hole mobility.
NET	:	Output vector from the Σ unit and input to the activation function of an ANN.
OUT	:	Output vector from an ANN.
r_o	:	Output resistance of MOSFET.
r_{od}	:	Output differential resistance.
r_{out}	:	Output resistance.
R_s	:	Sheet resistance.
T_{iC}	:	Conductance between input of the ith amplifier and output of the correction logic circuitry of a Hopfield A/D converter.
T_{ij}	:	Conductance between input of the ith amplifier and output of the jth amplifier of a Hopfield A/D converter.
T_{iR}	:	Conductance between input of the ith amplifier and reference voltage of a Hopfield A/D converter.
T_{iS}	:	Conductance between input of the ith amplifier and analog input voltage of a Hopfield A/D converter.
T_j	:	Equivalent conductance at the ith amplifier input node of a Hopfield A/D converter.
t_{PHL}	:	Propagation delay on transition from HIGH to LOW.
t_{PLH}	:	Propagation delay on transition from LOW to HIGH.
U_i	:	Voltage at the input of the ith amplifier.

V_i	:	Voltage at the output of the ith amplifier.
$V_{DS(sat)}$	:	Minimum drain-to-source voltage needed for saturation operation of a MOSFET.
V_{ID}	:	Differential input voltage.
v_N, V_N	:	Voltage applied to the inverting input terminal of the differential amplifier.
v_p, V_p	:	Voltage applied to the non-inverting input terminal of the differential amplifier.
V_R	:	Reference voltage.
V_s	:	Analog input voltage.
V_s^l	:	Lower limit of the analog input voltage to an A/D converter corresponding to a certain digital word.
V_s^u	:	Upper limit of the analog input voltage to an A/D converter corresponding to a certain digital word.
V_T	:	Threshold voltage.
V_{TRP}	:	Trip voltage.
W	:	MOS channel width.
$\mathbf{W}$	:	Weight vector of an ANN.
η	:	Training rate coefficient of an ANN.
$w_{PQ,k}$	:	Weight from neuron P in the hidden layer to neuron Q in the output layer k in a backpropagation ANN.
X	:	Input vector (matrix) to an ANN.

CONTENTS