AIN SHAMS UNIVERSITY
FACULTY OF ENGINEERING

# DIFFERENTIAL PASS TRANSISTOR LOGIC CIRCUITS



A thesis submitted to the Electronics and Communications Engineering Department in partial fulfillment for the degree of

MASTER OF SCIENCE



BY

**SOMIA ISMAIL KAYED**

under the supervision of

**PROF. HANI F. RAGAIE**

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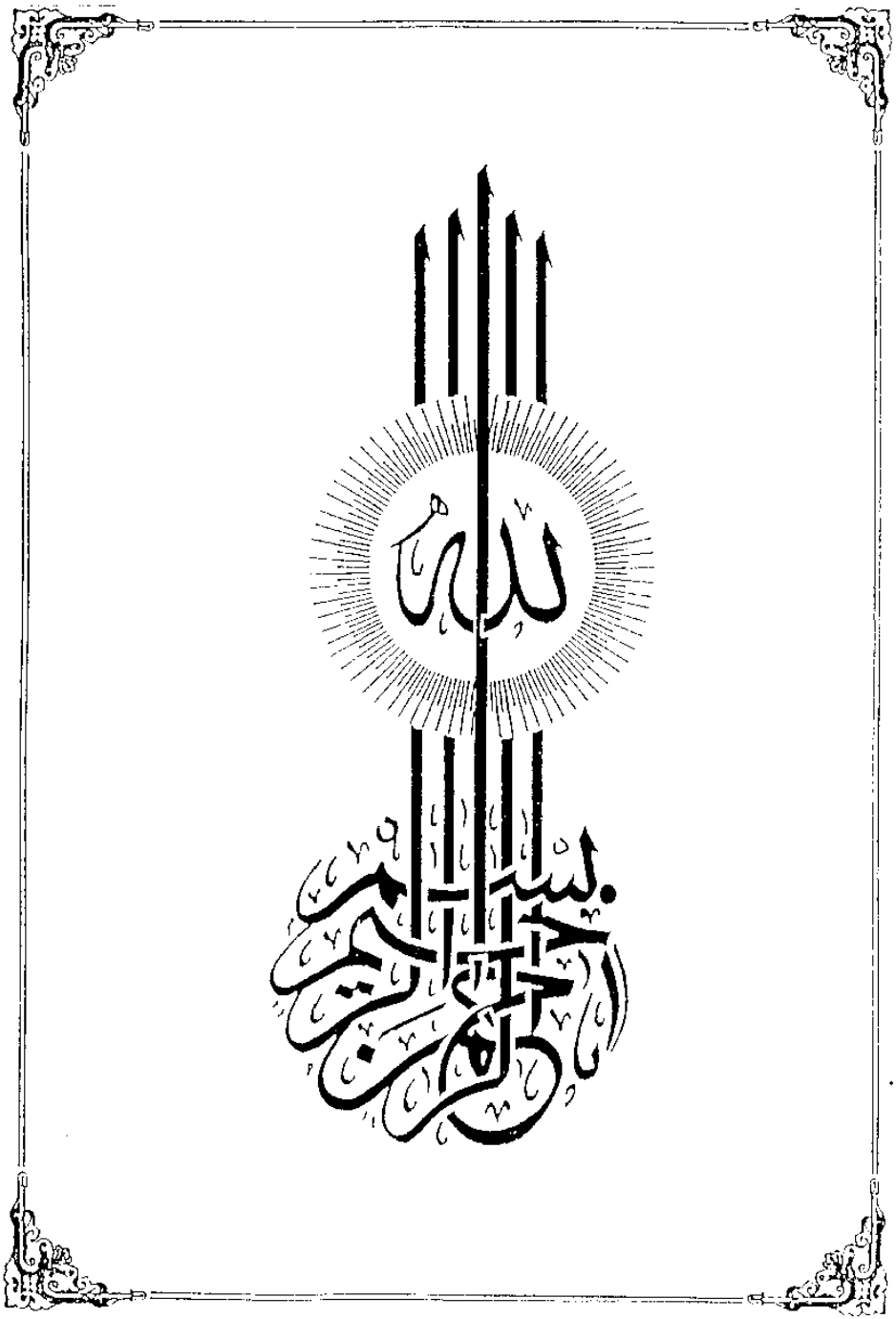

***TO MY FAMILY***

# STATEMENT

This dissertation is submitted to Ain Shams University for the degree of Master of Science in Electrical Engineering.

The work included in this thesis was carried out by the author in the Department of Communication & Electronic, Ain Shamas University.

No part of the thesis has been submitted for a degree qualification at any other University or institution.

Date : 26/3/96

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# ABSTRACT

**Name** : Somia Ismail Kayed

**Thesis title**: Differential Pass Transistor Logic Circuits

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**The n-type metal oxide semiconductor (NMOS) Pass-Transistor Logic (PTL) results in substantial area and speed improvements (0.5Ghz, 1800$\mu m^2$) compared to gate logic implementations (0.75Ghz, 2660$\mu m^2$). Conventional CMOS pass-transistor logic results in only moderate area and speed improvements when compared to CMOS gate logic.**

**In both NMOS and CMOS PTL techniques, however, the problem of noise immunity limits applications which suffer from relatively low logic swings. The high frequency switching of many densely-packed VLSI logic circuits produces significant noise. Noise voltages, typically induced in signal nodes by such mechanisms as capacitive coupling, can degrade system performance through increased logic settling times and even produce faulty circuit operation.**

**As a result, we need alternative pass-transistor configurations that directly address noise-immunity. Differential Pass Transistor Logic (DPTL) is a powerful configuration in CMOS technology. Its differential inputs is passed to the differntial outputs on condition of the control signal. The two differential outputs are used to drive differential buffers. SPICE simulations are used to compare conventional and differential logic on the basis of size and speed. Layouts are used to estimate area needed in both cases using the 2$\mu m$ technology. DPTL is the fastest (2.8 GHz) at all supply voltages including low voltage operations. The power-delay product, which is equivalent to the energy required to perform the needed function, is the lowest in DPTL implementations. Using the DPTL standard cell approach,**

**the universal, combinational, sequential, and computational circuits are implemented in 2μm technology.**

**Key words :**

**Pass transistor (PT), Transmission gate (TG), Differential Pass Transistor Logic (DPTL).**