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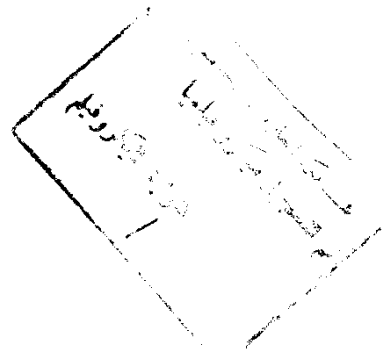
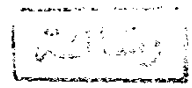


MODELING AND CHARACTERIZATION OF MICRONIC MOS TRANSISTORS



By

WAEL FIKRY FAROUK FIKRY ABD-ALLA

B.Sc. in Electrical Engineering & M.Sc. in Engineering Physics

A Thesis

Submitted in Partial Fulfillment for the Requirement of the Degree of

DOCTOR OF PHILOSOPHY

In

ENGINEERING PHYSICS

Department of Engineering Physics and Mathematics

Supervised By

Prof. Dr. O. A. Omar

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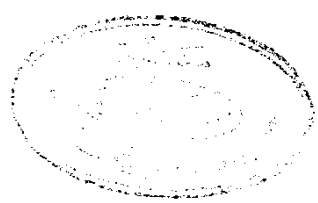

Cairo 1994

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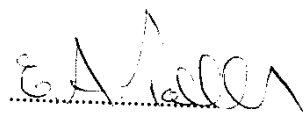

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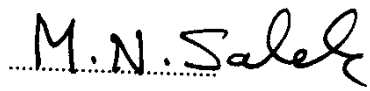

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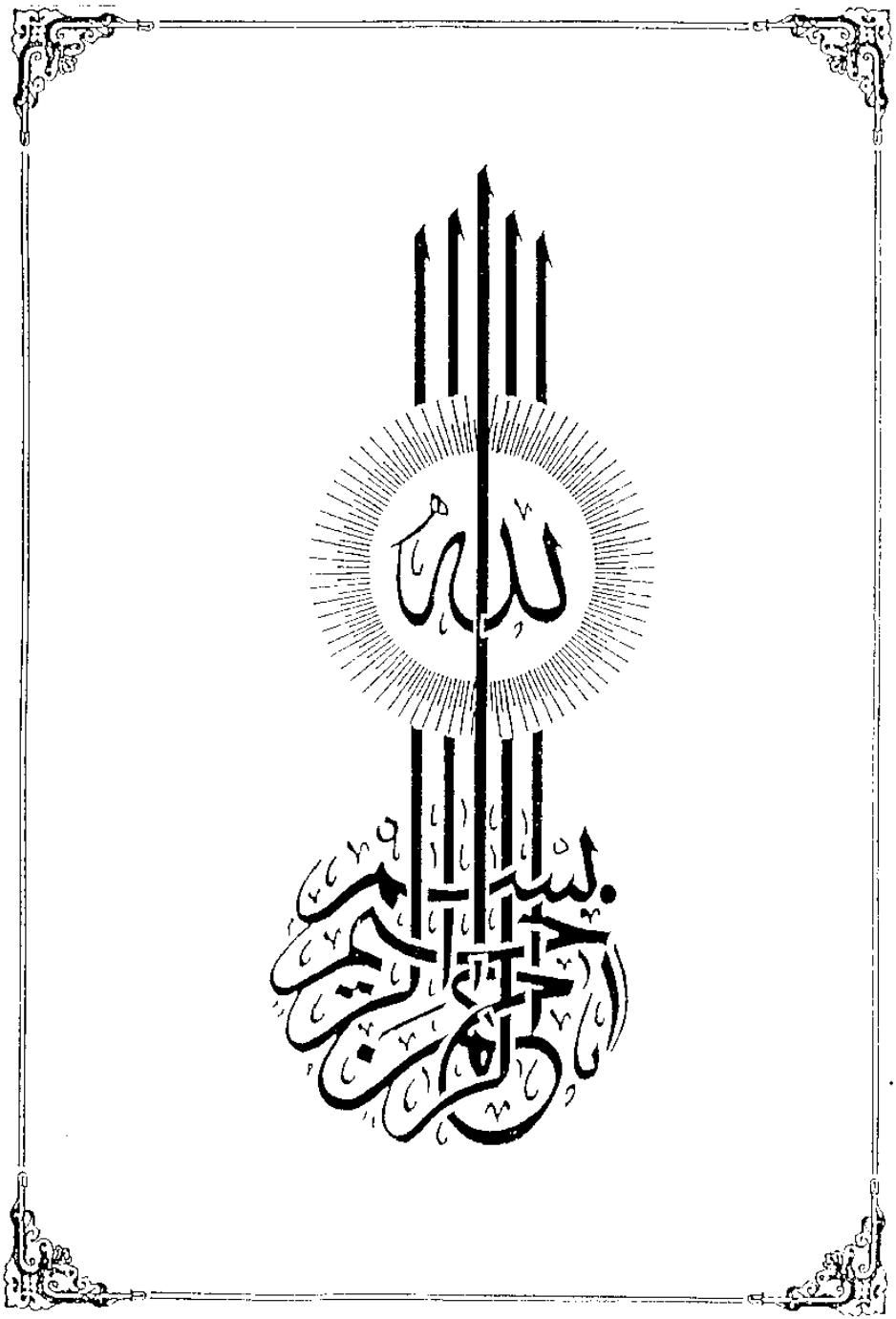

STATEMENT

This dissertation is submitted to Ain Shams University for the degree of Doctor of Philosophy in Engineering Physics.

The work included in this thesis was carried out by the author in the Department of Physics and Mathematical Engineering , Ain Shams University, from November 1989 to May 1994.

No part of this thesis has been submitted for a degree or a qualification at any other University or Institution.

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ABSTRACT

The main objective of the present work is to thoroughly study short channel and deep submicron MOS transistors through developing new techniques for the characterization of mobility, series resistance and short channel effects at room and low temperatures. A new approach is presented for the simultaneous determination of the effective channel mobility and the parasitic series resistance taking into account both vertical and lateral fields. The proposed method is applicable for short channel devices as well as for long channel ones. The method is based on the measurement of the dynamic transconductance, the gate-channel capacitance and the ohmic region drain current, all on a single transistor. The effective mobility and the electric field dependence are investigated at different temperatures. A study of the drain and transfer characteristics of the new generation of submicron n-channel MOSFET down to 0.1 μm is presented. The investigation is carried out using the two-dimensional numerical simulator "MINIMOS 4" to explain how the drain induced barrier lowering plays an important role in deep submicron device characteristics. Moreover, a novel method using the conductance and transconductance in the saturation region is proposed to determine the drain induced barrier lowering coefficient. The effect of temperature on the above mentioned characteristics down to 50 K is discussed. Then, a new method which takes into consideration the effects of the lateral field and saturation velocity is proposed to extract the deep submicron MOSFET parameters such as the threshold voltage, the effective channel length, the effective mobility and the parasitic series resistance.

LIST OF SYMBOLS

C_{bc}	Bulk-channel capacitance (F)
C_d	Depletion layer capacitance (F)
C_{gb}	Gate-bulk capacitance (F)
C_{gc}	Gate-channel capacitance (F)
C_{inv}	Inversion layer capacitance (F)
C_{ov}	Overlap capacitance (F)
C_{ox}	Gate oxide capacitance (F)
C'_{ox}	Gate oxide capacitance per unit area (F/cm^2)
d	Spacing between contact window and point of current crowding (cm)
E_c	Critical electric field (V/cm)
E_{eff} (E_y)	Effective vertical (normal) electric field (V/cm)
E_x	Lateral electric field (V/cm)
g_d	Drain conductance (S *or* mho)
g_m	Transconductance (S *or* mho)
I_d	Drain current (A)
I_g	Gate current (A)
I_S	Source current (A)
I_{Sub}	Substrate current (A)
J_n	Current density of electrons (A/cm^2)
J_p	Current density of holes (A/cm^2)
k	Boltzman constant (J/K)
L	Mask channel length (μm)
L_{eff}	Effective channel length (μm)

L_{win}	Contact window length (cm)
n	Density of free electrons (cm^{-3})
n_i	Intrinsic density (cm^{-3})
N_A	Acceptor impurity density (cm^{-3})
N_D	Donor impurity density (cm^{-3})
N_I	Ionized impurity density (cm^{-3})
p	Density of holes (cm^{-3})
q	Magnitude of electronic charge (C)
Q_B	Depletion (bulk impurity) charge density (C/cm^2)
Q_f	Fixed oxide charge density (C/cm^2)
Q_i	Inversion charge (C)
Q_{inv}	Inversion charge density (C/cm^2)
Q_{it}	Interface state charge density (C/cm^2)
r_d	Drain resistance (Ω)
r_s	Source resistance (Ω)
R_{co}	Contact resistance (Ω)
R_{sh}	Sheet resistance (Ω)
R_{sp}	Spreading resistance (Ω)
R_T	Series resistance (Ω)
S	Subthreshold Swing (mV/Decade)
S_n	Sensitivity of preamplifier (V/A)
T	Absolute temperature (K)
T_{ox}	Gate oxide thickness (nm *or* A°)
v_{sat}	Saturation velocity (cm/s)
V_b	Substrate voltage (V)
V_d	Drain voltage (V)

V_{dsat}	Drain saturation voltage (V)
V_{FB}	Flat band voltage (V)
V_g	Gate voltage (V)
V_t	Threshold voltage (V)
W	Mask channel width (μm)
W_{eff}	Effective channel width (μm)
X_{ac}	Distance between channel and starting point of current crowding(μm)
X_{dm}	Maximum depletion region width (cm)
X_{ch}	Channel thickness (μm)
X_j	Junction depth (μm)
ΔL	Lateral diffusion of the source and drain under the gate (μm)
∂L	Length of the pinchoff region (μm)
ε_{ox}	Silicon dioxide permittivity (F/cm)
ε_{si}	Silicon permittivity (F/cm)
η	Inversion charge weighting factor
θ	Mobility degradation factor (V^{-1})
λ	Drain induced barrier lowering coefficient
μ	Inversion layer (MOSFET) mobility (cm^2/V-s)
μ_B	Bulk mobility (cm^2/V-s)
μ_c	Coulomb scattering mobility (cm^2/V-s)
μ_{eff}	Effective mobility (cm^2/V-s)
μ_{FE}	Field-effect mobility (cm^2/V-s)
μ_n	Electron mobility (cm^2/V-s)
μ_{nI}	Electron ionized impurity scattering mobility (cm^2/V-s)
μ_o	Low field mobility (cm^2/V-s)
μ_p	Hole mobility (cm^2/V-s)

μ_{pl}	Hole ionized impurity scattering mobility (cm^2/V-s)
μ_{ph}	Phonon scattering mobility (cm^2/V-s)
μ_S	Surface mobility (cm^2/V-s)
μ_{sat}	Saturation mobility (cm^2/V-s)
μ_{sr}	Surface roughness scattering mobility (cm^2/V-s)
ρ	Resistivity (Ω cm)
ρ_c	Contact resistivity (Ω cm^2)
ρ_s	Sheet resistance per square ($\Omega/\square$)
ϕ	Electrostatic potential (V)
ϕ_p	Surface potential at pinchoff (V)
ϕ_f	Bulk fermi potential (V)
ψ_s	Surface potential (V)

Abbreviations

CLM	Channel Length Modulation
DIBL	Drain Induced Barrier Lowering
HCE	Hot Carrier Effect
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
ULSI	Ultra Large Scale Integration
VLSI	Very Large Scale Integration

CONTENTS

INTRODUCTION