MEASUREMENT OF INTERFACE STATES IN MOS DEVICES HAVING DIFFERENT OXIDE THICKNESSES

A THESIS

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This thesis

on

"Measurement of interface states in MOS devices having different oxide thicknesses"

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SUMMARY

The main purpose of this work is to establish a local MOS technology.

This research offers a complete study of the MOS capacitor characteristics as it is the most useful device in characterizing the technology.

The thesis consists of four chapters:

@ The first chapter is a review of MOS capacitor theory. It includes the capacitance-voltage characteristics of the Ideal MOS capacitors and the parameters that affect these characteristics in real MOS capacitors.

The second chapter describes briefly the methods of measuring the device parameters. e.g. interface states. fixed oxide charge. doping and monitoring carrier lifetime.

@ Experimental work on technology and measurement techniques are presented in the third chapter. A typical set of results for each method is given. and the limitations of each measurement setup are discussed.

@ The dependence of device parameters on some technological processes is discussed in the fourth chapter. Physical explanation of such dependence and the limitations of our established technology are given.

LIST OF SYMBOLS

A	Area of the MOS capacitor,cm^{2}
B	Parabolic rate constant for thermal oxidation,$nm^{2}.min^{-1}$
B/A_{o}	Linear rate constant for thermal oxidation,nm.min
C	MOS capacitance ,$F.cm^{-2}$
C_{a}	Accumulation capacitance,$F.cm^{-2}$
C_{d}	Depletion capacitance,$F.cm^{-2}$
C_{FB}	Flat band capacitance,$F.cm^{-2}$
C_{i}	Inversion capacitance,$F.cm^{-2}$
C_{sc}	Semiconductor space charge capacitance,$F.cm^{-2}$
C_{ss}	Interface states capacitance,$F.cm^{-2}$
$C(min)$	Minimum high frequency capacitance,$F.cm^{-2}$
$C(final)$	Final high frequency capacitance when a voltage step is applied to force the capacitor from strong accumulation to strong inversion, $F.cm^{-2}$
d_{ox}	Oxide thickness,nm
F_{BD}	Breakdown field,$MV.cm^{-1}$
E_{c}	Conduction band energy level,eV
E_{F}	Fermi level,eV
E_{FB}	Fermi level in the bulk of the semiconductor,eV
E_{Fs}	Fermi level at the surface of the semiconductor,eV
E_{g}	Energy difference between the conduction band and the valence band,eV
E_{i}	Intrinsic Fermi level,eV
E_{s}	Electric field at the semiconductor surface,$V.cm^{-1}$

I_d	Depletion current, A
I_g	Gate current, A
I_{gen}	Generation current, A
I_g	Current related to the flow of the inversion charge from the interface to the bulk of the semiconductor, A
K	Boltzman constant, $J.°K^{-1}$
L_D	Extrinsic Debye length for n-type semiconductor, cm
N_D	Density of donor impurities, cm^{-3}
N_{ss}	Interface states density, $eV^{-1}.cm^{-2}$
n_i	Intrinsic carrier concentration, cm^{-3}
n_n	Electron density in the conduction band in an n-type material cm^{-3}
n_{no}	Equilibrium electron density in the conduction band in an n-type material, cm^{-3}
p_n	Holes density in the valence band in an n-type material cm^{-3}
p_{no}	Equilibrium holes density in the valence band in an n-type material, cm^{-3}
Q_d	Depletion charge, $C.cm^{-2}$
Q_g	Gate charge, $C.cm^{-2}$
Q_i	Inversion charge, $C.cm^{-2}$
Q_{ox}	Fixed oxide charge, $C.cm^{-2}$
Q_{sc}	Semiconductor space charge, $C.cm^{-2}$
Q_{sc}	Interface states charge, $C.cm^{-2}$
q	Electron charge, C
R_c	resistance associated with the exchange of electrons between the interface states and the conduction band, $\Omega.cm^{-2}$

R_g	Resistance associated with the generation and recombination within the depletion layer, $\Omega.cm^{-2}$
R_{ss}	Resistance arises from the loss due to capture and emission of carriers by interface states, $\Omega.cm^{-2}$
R_v	Resistance associated with the exchange of holes between the interface states and the valence band, $\Omega.cm^{-2}$
S_o	Surface recombination velocity,$cm.sec^{-1}$
T	Temperature,°C
T_o	Relaxation time of the MOS capacitor when a small step is applied, μsec
t	Time,sec
U_g	Minority carrier generation rate, $cm^{-3}.sec^{-1}$
V_{FB}	Flat band voltage,V
V_g	Gate voltage,V
V_{ox}	Voltage drop across the oxide,V
X	Distance into the semiconductor , cm
X_d	Depletion layer width,cm
X_{dss}	Steady state depletion layer width,cm
$X_d(max)$	Maximum width of the depletion layer,cm
X_o	Pregenration depletion layer width,cm
α	Ramp rate,$V.sec^{-1}$
ϵ_{ox}	Oxide dielectric constant,$F.cm^{-1}$
ϵ_s	Semiconductor dielectric constant,$F.cm^{-1}$
ϕ_m	Metal work function,eV
ϕ_s	Semiconductor work function,eV
ϕ_{ms}	Metal-semiconductor work function difference,eV
χ	Electron affinity in the semiconductor,eV

ρ	Charge density in the semiconductor, $C.cm^{-2}$
τ	Minority carrier generation lifetime, μsec
τ_i	Inversion layer formation time constant, sec
τ_{ss}	Interface state time constant, sec
Ψ	Potential difference in the semiconductor, V
Ψ_B	Potential difference in the bulk of the semiconductor, V
Ψ_s	Surface potential difference, V
Ψ_{so}	Berglund's constant (surface potential at strong inversion), V

INTRODUCTION

The main purpose of this work is to establish an MOS technology suitable for the available infra structure of our laboratory. To establish such a technology, specific measurement setups are needed for appropriate characterization.These include the dynamic MOS cpacitance versus gate voltage at high and low frequencies, the transient response of the capacitor and non equilibrium capacitance characteristics. The main three parameters that characterize the technology are:

1- The fixed oxide charge per unit area.

2- The interface states density and their energy distribution.

3- The minority carrier lifetime.

The dependence of these parameters on technological processes is determined in order to fix the limits of the established technology This has been carried out by measuring the parameters of thermally grown oxide of different thicknesses. Oxides having thicknesses between 100 nm and 20 nm have been fabricated using a dry oxidation process.

The thesis consists of four chapters:

The first chapter is a review of MOS capacitor theory. It includes the capacitance-voltage characteristics of the ideal MOS capacitors and the parameters that affect these characteristics in real MOS capacitors.

The second chapter describes briefly the methods of measuring the device parameters.e.g. interface states,fixed oxide charge,flat band voltage,doping and minority carrier lifetime.

The third chapter deals with the technological processes used in the fabrication of MOS capacitors. These processes are wafer cleaning, thermal oxidation, metallization, photolithography and annealing. This is followed by the measurement techniques used. A typical set of results are given and the limitations of each measurement setup are discussed.

Results are analyzed in the fourth chapter in order to find the dependence of device parameters on some technological processes. Problems encountered and proposed solutions are presented. The breakdown characteristics are studied and the limitations of our established technology are fixed.

All technological and characterization steps given in this work have been carried out at the integrated circuits laboratory of the Electronics and Computer Department, Faculty of Engineering Ain Shams University.

CHAPTER (1)