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Modeling and Simulation of Digital Circuit in VHDL and PSpice:

a Comparative Study

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STATEMENT

This dissertation is submitted to Ain Shams University in partial fulfillment of the requirments for the degree of Master of Science in Electrical Engineering (Computer and System Engineering).

The work included in this thesis was carried out by the author at Computer and Systems Engineering Department, Ain Shams University.

No part of this thesis has been submitted for a degree or a qualification at any other universities or institutions.

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ABSTRACT of M.Sc Degree

On

Modeling and Simulation of Digital Circuit in VHDL and PSpice a Comparative Study

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Using hardware description languages in Modeling and simulation of hardware systems is an important and challinging subject. Several computer languages are devised especially for this task with some successes and failures.

The aim of this research is to investigate the capabilities and limitations of two famous hardware description languages. Brief description of both (VHSIC Hardware Description Language) VHDL and (Simulation Program with Integrated Circuit Emphasis) PSpice are addressed. The basic digital building blocks are described and simulated using the two languages. A compraison between the two models (VHDL model and PSpice model) of each building block is performed and explained, as well as the limitations of both languages are described.

A real case study (Priority switch circuit) is performed to verify the results of the comparison between the two languages. The circuit is descriped using these primitives in both languages. The two models are simulated using a digital and mixed mode simulators. The results confirm that capability of VHDL in modeling and simulation of digital circuits however the PSpice is more powerful in analog simulation.

key words

VHDL, PSpice, Modeling and Simulation.



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