DESIGN AND REALIZATION
OF A LOW LEVEL CURRENT TO FREQUENCY CONVERTER
(1E – 13A TO 1E – 8A)

A THESIS

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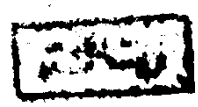

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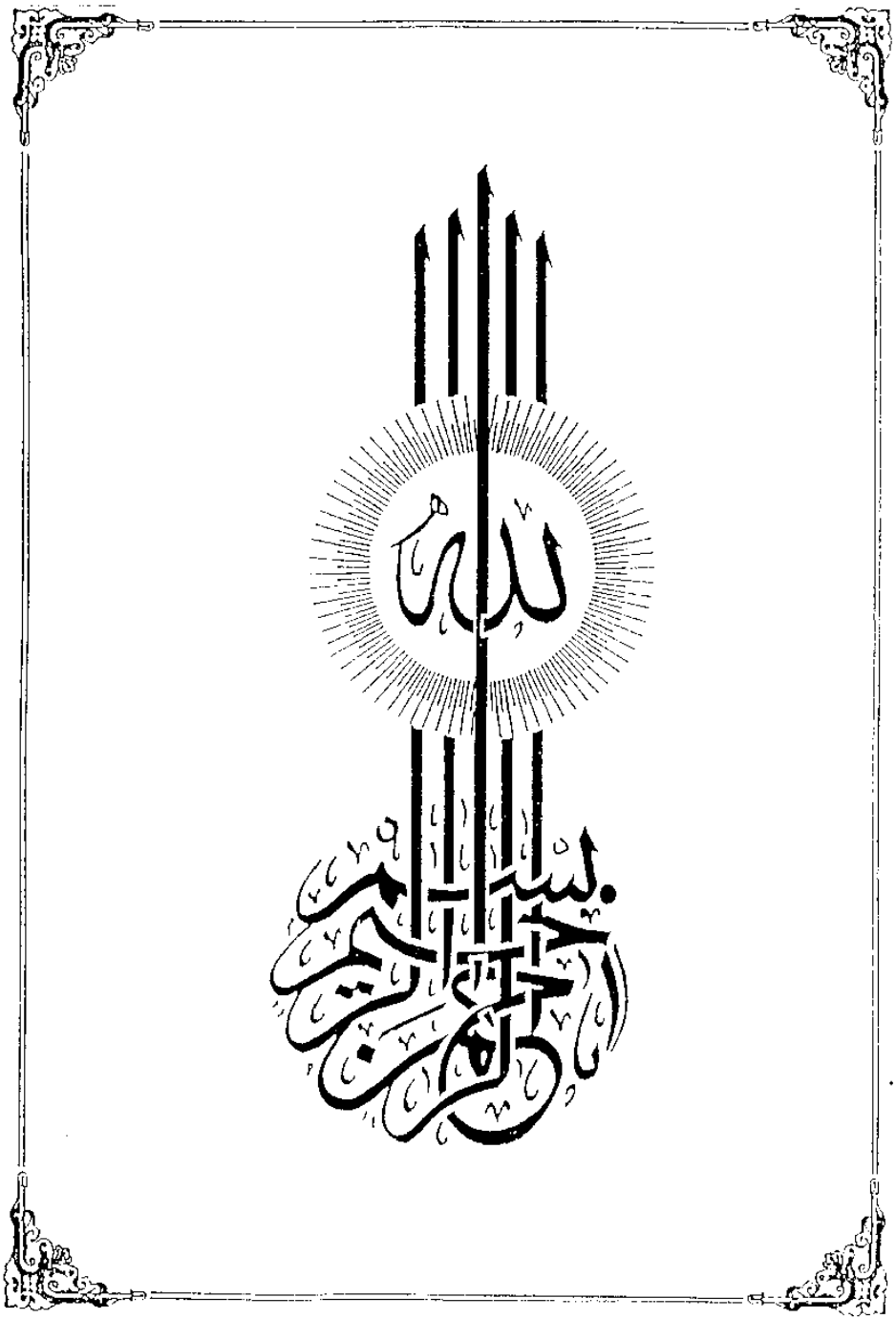

SUMMARY

The very low level current measurement (1 E(-13A) requires a high input impeadance amplifier,generally using an unprotected MOSFET and a high value resistor (=1E12 ohm). An improved current to frequency converter (CFC) fully integrated in NMOS technology is presented in this thesis. This converter uses the switched capacitor technique. This version is characterized by better topology of devices, wider dynamic range of frequency and the incooperation of circuitry that detects the saturation of the 1/F characteristics and then enforces a range change which effectively moves the current measurement points towards the linear portion of the characteristics.

In CHAPTER 1, we recall the MOS processing (material, oxidation, diffusion, masking, etching, scribing and fabrication), structure and characteristics. We also intoduce a formulation of the MOSFET capacitor in its different modes of operation.

We present also in this chapter the methods of very low level current measurements, the different sources of leakage currents in MOS devices and the precautions to be considered for the compensation or the minimization of this leakage which enables the very low level current measurements at a very good resolution accuracy and linearity.

In CHAPTER 2, we explain a new accurate, sensitive and linear current to frequency converter (CFC) and present a detailed study of the analysis and design considerations for the different blocks constructing it. We have proposed models for predicting the performance and characterizing these building blocks. These models take into account all restrictions and limitations associated with the MOSFET VLSI

circuits. These models are very important for the study and the treatment of some nonlinearity problems revealed from comparing the theory and experimental results. However, our simulation results show that the CFC which we have presented properly functions at very good linearity and accuracy.

In CHAPTER 3, we introduce the different precautions to be considered when preparing the test samples,to guarantee the lowest possible level of leakage current during measurements. We present our results of simulation, discuss and compare it with experimental results performed on an old version of CFC. Our results revealed that:

a) Lower limit of current measurement is related to the uncompensated leakage current created at the input of the current controlled oscillator,

b) The suplementary current is related to the proximity effect,

c) The frequency jump in the CFC transfer function is not related to the OPAMP oscillation due to instability as was beleived to be, but is related to the threshold voltage instability of the MOSFET's used in the I/F resistance and,

d) Frequency saturation of the CFC characteristics is not related to the deviation from the exponential c/c's of the exponential current generator, but is related to the relatively long delay of the double bistable multivibrator used in the current controlled oscillator.

We finally propose :

a) Using low leakage MOSFET techniques,

b) Using deposied and diffused guard rings between the channel of the first MOSFET and the source of the second MOSFET used in the R(F) resistance,

c) New techniques to compensate for the carrier heating in the R(F) resistance and,

d) the use of more advanced technology (CMOS, MOS/SOS or CMOS/SOS).

LIST OF CONTENTS

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CHAPTER I

MOSFET STRUCTURE, PROCESSING AND DIFFERENT TECHNIQUES OF LOW LEVEL CURRENT MEASUREMENTS

Introduction

An improved current to Frequency Converter (CFC) fully integrated in NMOS technology is presented in this thesis. We first recall the MOSFET structure, characteristics and processing. We also formulate the MOS capacitor in the different modes of operation.

We study afterwards the different sources of leakage in MOS devices (oxide bulk, oxide boundaries, oxide surface and junction leakage currents) and explain the precautions to be considered for the compensation or the minimization of these leakage currents ($< 10^{-15}$ A). These precautions make it possible to measure the very low level currents at a very good resolution, accuracy and linearity. We finally present new techniques compatible with the MOSFET technology and the scaling down trends for measuring the very low level currents. This study is very important for :

a) The choice of the optimal method to be used for the leakage compensation.

b) Enlarging as possible the dynamic range of measurement.

c) The improvement of the device sensitivity, resolution and linearity.

d) obtaining the best quality to price ratio.

e) Improvement of the device reliability and reproducibility.

1.1 MOSFET STRUCTURE AND CHARACTERISTICS

The metal-oxide-semiconductor field effect transistor or MOSFET consists as shown in fig. (1-1) of: Source S, drain D and gate G. The gate electrode is separated from the channel by a thin layer of SiO_2. p and N type channel MOSFET's are commercially available. As will be shown below, the N-type is of great commercial importance. Depending on the mode of operation we can classify the MOSFET into two families:

Enhancement mode EMOSFET and,
Depletion mode DMOSFET .

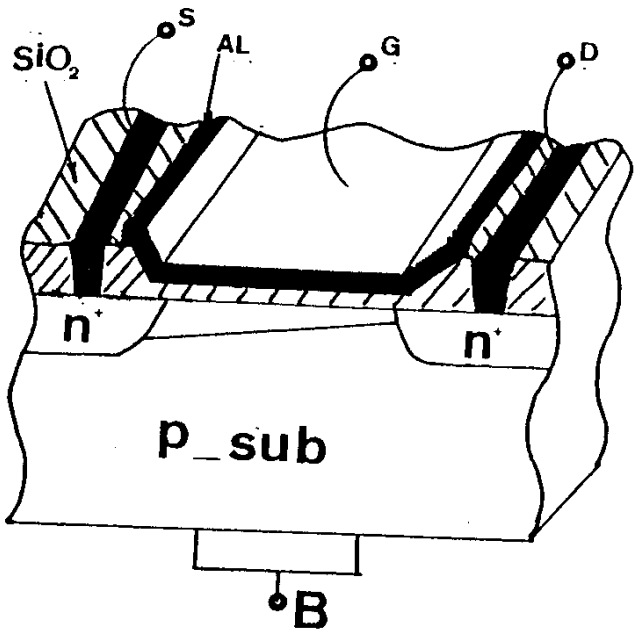


FIG.(1-1 A)

EMOSFET STRUCTURE

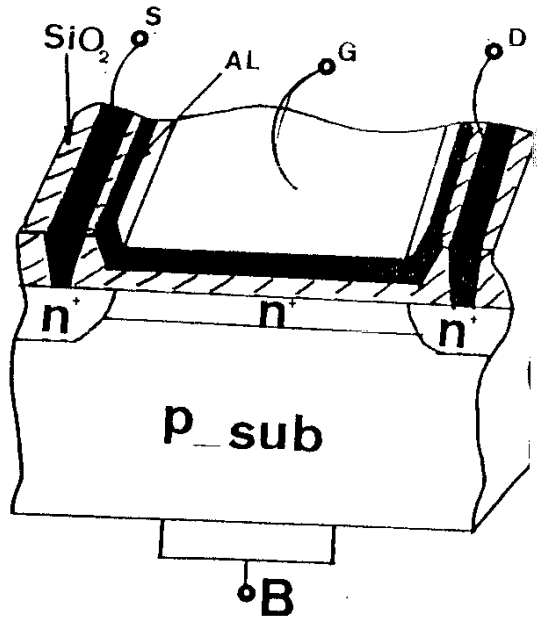


FIG.(1-2 A)

DMOSFET STRUCTURE

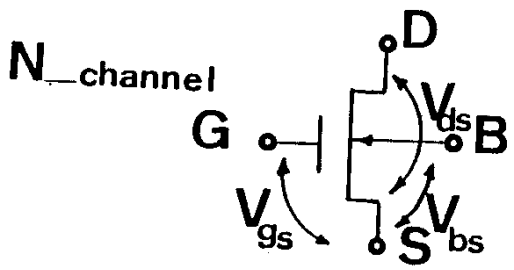
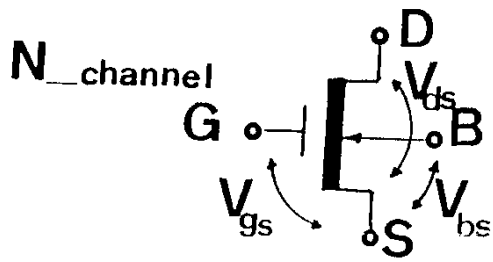


FIG.(1-1 B)

EMOSFET SYMBOL



FIG(1-2 B)

DMOSFET SYMBOL

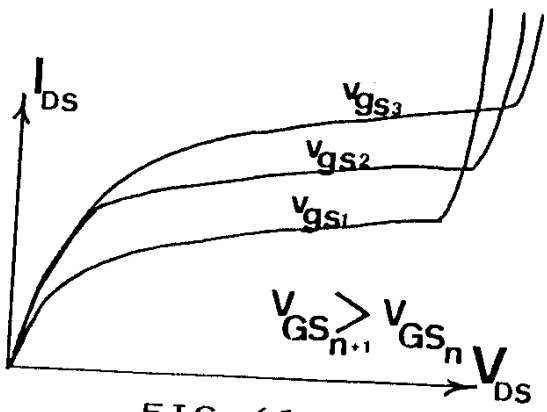


FIG.(1-1 C)

EMOSFET CHARACTERISTIC

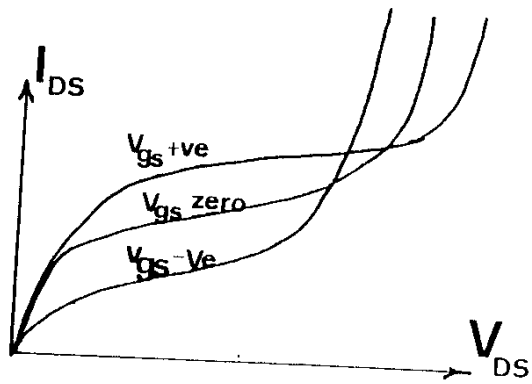


FIG.(1-2 C)

DMOSFET CHARACTERISTIC

In Fig.(1-1)(N-type EMOSFET), a conducting channel is created between the source and the drain by the gate voltage; an induced electric field is established between the gate and the P-type substrate perpendicular to the Si-SiO_2 interface. With a small positive gate voltage,holes in the adjacent P-material are repelled out and a depletion layer is formed. At a slightly more positive voltage, an inversion layer of mobile electrons is formed. The surface conductivity has then been "enhanced", and the transistor is there - fore "turned on", and current can flow between source and drain.

In the DMOSFET , a thin lightly-doped conducting layer is implanted into the channel region (see Fig.(1-2. a)). In the absence of gate voltage, the channel is conducting and the MOSFET is on. When the gate is biased by a positive voltage, the channel conductivity is enhanced and a grea - ter current is then allowed to flow from the source to drain. The contrary is true when biasing the gate by a negative voltage. This can be shown in Fig. (1-2. c). The symbol of the DMOSFET is shown in Fig. (1-2. b) . We observe that the characteristic curves of the DMOSFET are similar to those for the EMOSFET with the added flexibility of permitting positive or negative control gate voltages.

The MOSFET current I_{Ds} is related to the drain, gate and threshold voltages V_{Ds} , V_{Gs} and , V_T respectively, in the different regions of opera - tion , by :

$$I_{Ds} = \mu C_{ox} \frac{Z}{L} \left[(V_{Gs} - V_T) V_{Ds} - \frac{V_{Ds}^2}{2} \right], \quad V_{Ds} < \left| V_{Gs} - V_T \right|$$

$$I_{Ds} = \mu C_{ox} \frac{Z}{L} \frac{[V_{Gs} - V_T]^2}{2(1 - \frac{\Delta L}{L})}, \quad V_{Ds} \geq \left| V_{Gs} - V_T \right| \qquad (1\text{-}1)$$

where

Δl is the pinch off region length given by:

$$\Delta l = k \left[\frac{V_{Ds}}{V_{Gs} - V_T} - 1 \right]^{2/3}$$

$$k = \left[\frac{9}{4} \frac{L \, d_o \, h_{ox} \, \epsilon_s}{\epsilon_{ox}} \right]^{1/3}$$