AIN SHAMS UNIVERSITY

FACULTY OF ENGINEERING

MODELING AND PERFORMANCE EVALUATION OF MICROPROCESSOR ARCHITECTURES

A THESIS
SUBMITTED IN PARTIAL FULFILLMENT
OF THE REQUIREMENTS OF
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(COMPUTER & SYSTEMS ENG.)

BY

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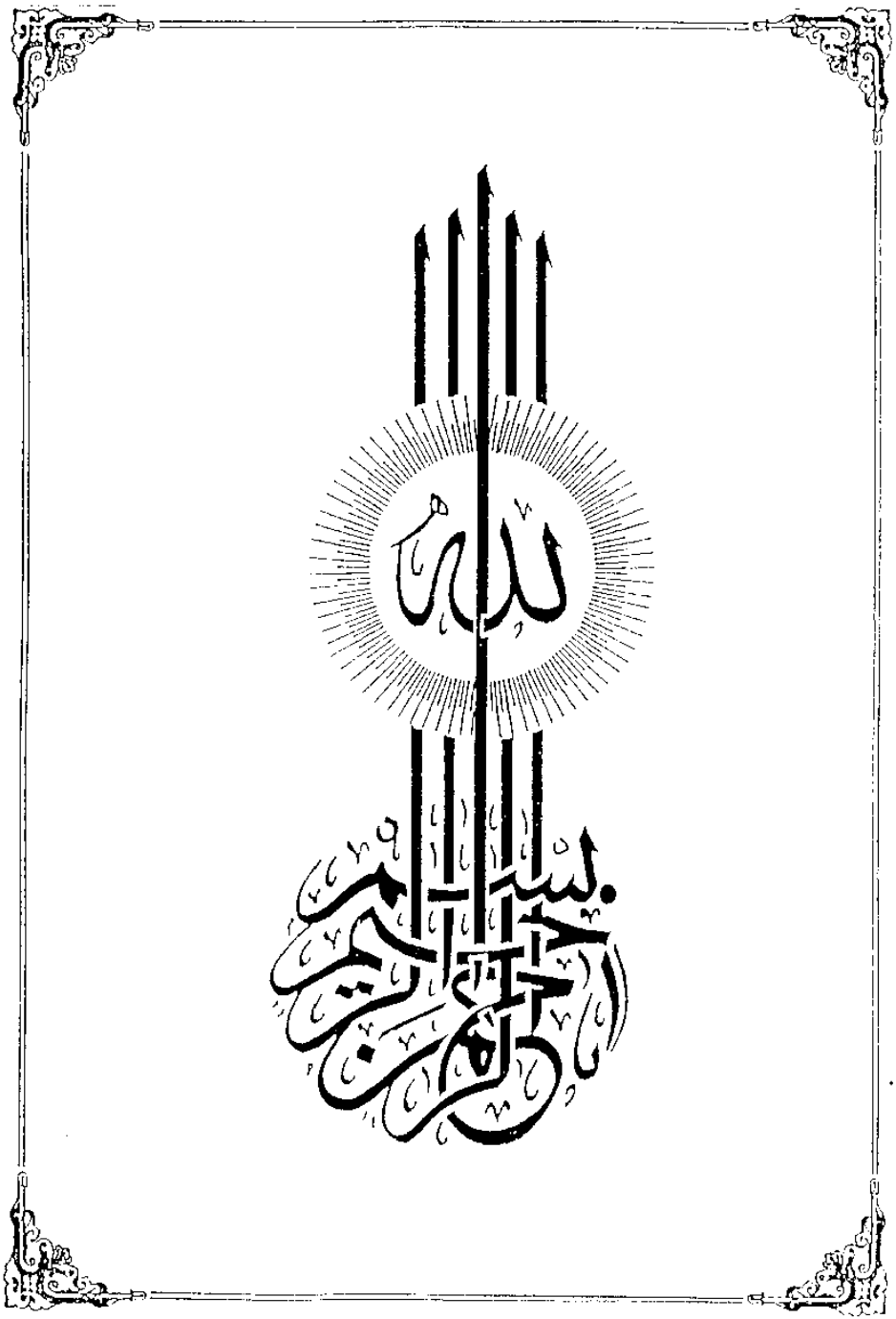

EXAMINERS COMMITTEE

The undersigned certify that they have read and recommend to the faculty of Engineering , Ain Shams University for acceptance a thesis entitled " MODELING AND PERFORMANCE EVALUATION OF MICROPROCESSOR ARCHITECTURES " submitted by ENG. MANAL ABDEL AZIZ ALY in the Computer and Systems Engineering for the degree of Master of Science in Computer Engineering.

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جامعة عين شمس
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ملخص رسالة الماجستير المقدمه من المهندسه / منال عبد العزيز على

العنوان : نمذجة وتقييم الاداء بالنسبه لبنية الميكروحاسبات

تحت اشراف : أ.د. محمد أديب رياض غنيمى

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ملخص الرساله :

يختص هذا البحث بالدراسه والتحليل لكيفية مواءمة حمل تشغيل معين لنوع من الميكروحاسبات وذلك للحصول على أفضل أداء ممكن .

ولهذا الغرض كان تتابع البحث كالتالى :

١ - دراسة للانواع المختلفه من الميكروحاسبات وتوضيح مدى مناسبتها للتطبيقات المختلفه وانعكاس ذلك على بنيه هذه الميكروحاسبات .

٢ - دراسة أسس نمذجة الميكروحاسبات على المستويات المختلفه وتطبيق ذلك على نوع عام من الميكروحاسبات كمثال .

٣ - دراسة طرق تقييم الاداء للميكروحاسبات وكيفية قياسها والحصول عليها من النموذج المعد .

وقد تم استخدام نظم المحاكاه لتمثيل النماذج وطرق الاداء السابقه على الحاسب. كما تم استخدام حزمة Network II.5 كأداه لنظم المحاكاه حيث تسمح هذه الحزمه بسهوله تغيير بعض المؤشرات فى النموذج السابق وقياس بعض قياسات الاداء المعنيه .

أسلوب تقييم الاداء فى هذا البحث يمكن تلخيصه باستخدام ثلاثة نماذج رئيسيه : نموذج بنيه الميكروحاسب (HW) ، ونموذج برنامج التحميل (SW) ، ونموذج الاداء.

نموذج بنيه الميكروحاسب يشير الى مجموعة القواعد والعروض التى تمثل مكونات البنيه الاساسيه للميكروحاسبات فى النموذج المستخدم .

أما نموذج برنامج التحميل فهو عباره عن وصف لمعيار برنامج التحميل لاختبار بنيه الميكروحاسب المستخدم ، وكذلك كيفية التعبير عن هذا البرنامج بصوره تتفق مع طريقة تقييم الاداء المستخدمه .

نموذج الاداء يصف مجموعه من قياسات الاداء وكذلك مؤشرات الاداء المستخدمه لاختبار بنية الميكروحاسب السابق .

Ain Shams University
Faculty of Engineering
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M.Sc. Thesis suhmitted by: Eng./Manal Abdel Aziz aly
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superuisors: 1- Prof. M.A.R.Ghonaimy
2- Dr. Nashaat El-Khameesy
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Research Summery

This research is concerned with study and analysis of how to match a workload onto a microprocessor to enhance performance. For this purpose, the sequence of research is as follows:

1- Study and analysis of different types of microprocessors indicating its suitability for different applications and how this is reflected on its architectures.
2- Study the basis for modeling microprocessor at different levels and apply this on a general purpose microprocessor(Transputer) as an example.
3- Study methods for performance evaluation of microprocessors and how to measure and obtain it from the model.

Simulation was used to represeut the model and its performance in the computer. In this research, we used the Network II.5 as a simulation tool. Network II.5 permits a flexible change in the model parameters to measure some performance metrics.

The evaluation methodology can be summerized in terms of three main attributes. These are: hardware model, and performance model.

First, the hardware model refers to the set of assumptions, rules and methods of represeuting the physical hardware components into a studied model.

Second, the software model is a description of a specific criterion defining which software programs should be used to test the hardware, as well as defining how such sw. benchmarks are mapped into a form compatible to the user for evaluation.

Third, is the performance model which defines the set of performance metrics as well as any targeted performance parameters of the tested Hw.

STATEMENT

This thesis is submitted to Ain Shams University for the Degree of Master of Science in Computer Engineering.

The work included in this thesis is carried out by the author in Department of Computer and Systems Engineering , Ain Shams University.

No part of this thesis has been submitted for a degree or a qualification at any other University or Institution.

Date : ١/١١/١٩٩٢

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ABSTRACT

Throughout this thesis a number of problems regarding the performance evaluation of microprocessors have been encountered; along a targeted model of the Transputer. These include the limitations associated with analytical queuing modelling when the too complex interaction between the different hardware resources exist .

Secondly, the problem of developing a flexible evaluation model which avoids the common problems with current benchmarks being biased to a certain architecture other than the other.

Consequently, this research has conducted an indepth study covering the recent architectural trends and performance evaluation techniques . A flexible evaluation model has been developed of three major attributes ; the hardware (HW) ; the software (SW) ; and the performance . In this model the HW-model presents an easily modifiable simulation model for the Transputer at the micro - architecture level . The SW-model is the mapping model to the workload activities being translated according to the simulation instruction of the HW-model . A number of

performance metrics including execution time, speed up gain, utilization, average instruction time, bus traffics, and memory request weight have been defined for evaluation. The performance model has established an evaluation criterion based on the correlation between the simulation results of a number of modifications made on the actual reference model .

The work done in this research while tries proven and verified evaluation methodology that can be employed on similar processor; has also come up with other contributions . A number of possible enhancements in the Transputer architecture has been examined along its effects on the overall performance of the current Transputer design . Results have proven that both the serial-link (SL) and the main processor (MP) components are the critical items for enhancements . A speed up of 10 - 15 times the cycle time of the MP as well as 3 times the band width of the SL would raise the overall performance figures by a factor of 2 . Investments in other components have not proven well justified performance gain . Balanced utilization of different components has also been measured yielding the recommendation of a bounded computational to input/output ratio between 40% - 60% .

CONTENTS

CHAPTER III : PROBLEM FORMULATION

CHAPTER IV : MODEL DESCRIPTION

CHAPTER V : THE RESULTS