



شبكة المعلومات الجامعية

بِسْمِ اللَّهِ الرَّحْمَنِ الرَّحِيمِ

جامعة عين شمس

شبكة المعلومات الجامعية

@ ASUNET



شبكة المعلومات الجامعية

جامعة عين شمس

التوثيق الالكتروني والميكرو فيلم

قسم

نقسم بالله العظيم أن المادة التي تم توثيقها وتسجيلها
علي هذه الأفلام قد أعدت دون أية تغييرات



يجب أن

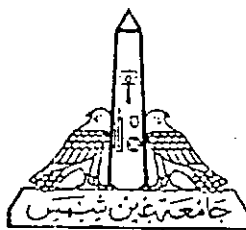
تحفظ هذه الأفلام بعيدا عن الغبار

في درجة حرارة من 15-25 مئوية ورطوبة نسبية من 20-40%

To be Kept away from Dust in Dry Cool place of
15-25- c and relative humidity 20-40%



شبكة المعلومات الجامعية التوثيق الالكتروني والميكروفيلم



Ain Shams University
Faculty of Engineering
Electronics and Communications Engineering Department

VHDL Synthesis for ASICs
Applied to DLX RISC Processors

A Thesis

Submitted in Partial Fulfillment of the Requirement
for the Degree of Master of Science
in Electrical Engineering

Submitted by

Ibrahim Al-Hanafy Al-Mohandes
B.Sc. in Systems and Computer Engineering,
Al-Azhar University, 1994

Supervised by

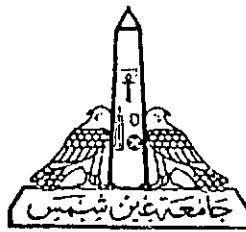
Prof. Dr. Hany F. Ragaie Prof. Dr. Mohamed K. El-Said
Prof. Dr. Ali M. Rashed

Cairo 1998

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بِسْمِ اللَّهِ الرَّحْمَنِ الرَّحِيمِ

To my parents,
my brother, and my sisters

Examiners Committee

Name Ibrahim Al-Hanafy Al-Hanafy Al-Mohandes

Thesis VHDL Synthesis for ASICs Applied to DLX RISC Processors

Degree Master of Science in Electrical Engineering

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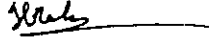
STATEMENT

This dissertation is submitted to Ain Shams University for the degree of Master of Science in Electrical Engineering (Electronics and Communications Engineering).

The work included in this thesis was carried out by the author at the Electronics and Communications Engineering Department, Faculty of Engineering, Ain Shams University.

No part of this thesis was submitted for a degree or a qualification at any other university or institution.

Date : / /1998

Signature : 

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