

AIN SHAMS UNIVERSITY FACULTY OF ENGINEERING

Electronics and Communications Engineering Department

A Delta-Sigma Fractional-N frequency synthesizer

A Thesis

Submitted in Partial Fulfillment of the Requirements

For the Degree of Master of Science in Electrical

Engineering

(Electronics and Communications Engineering)
Submitted By

Eng. Rana Aly Onsy Abd El Salam

Supervised By

Prof. Adel E. El-Hennawy Dr. Mohamed Mohamed El Nozahi

> Cairo – Egypt 2012

STATEMENT

This dissertation is submitted to the Faculty of Engineering, Ain Shams University for the degree of Master of Science in Electrical Engineering (Electronics and Communications Engineering).

The work included in this thesis was carried out by the author at the Electronics and Communications Department, Faculty of Engineering, Ain Shams University, Cairo, Egypt.

No part of this thesis was submitted for a degree or a qualification at any other university or institution.

Name: Rana Aly Onsy Abd El S	alam
Signature:	
Date:	



Name: Rana Aly Onsy Abd El Salam

Thesis Title: Delta-Sigma Fractional-N frequency synthesizer

Degree: Master of Science dissertation, faculty of Engineering, Ain

Shams University, 2012

ABSTRACT

In this thesis, a Delta-Sigma Fractional-N frequency synthesizer using a phase selection approach is designed. This approach aims at decreasing fractional spurs that appear when using fractional-N frequency synthesizers. The phase selection approach is a method to carry out fractional division by toggling between different fractional division ratios. The average of these fractional division ratios is equal to the required fractional division ratio. Eight signals, shifted in phase by $\frac{\pi}{4}$, are generated from the output of the frequency synthesizer using a phase generator. Each reference cycle, a fractional division ratio is achieved by selecting one of the eight signals. A MASH 1-1-1 Delta-Sigma modulator is used to control the phase selection process. The difference between two successive fractional division ratios at two successive reference cycles corresponds to the difference between two successive output values of the Delta-Sigma modulator at the same reference cycles.

This approach was designed using 130nm TSMC design kit and a supply voltage of 1.5 volts. It was able to achieve better results than those

of the conventional fractional-N frequency synthesizers regarding phase noise and fractional spurs.

Key Words:

Fractional-N frequency synthesizer, integer-N frequency synthesizer, MASH 1-1-1 Delta-Sigma modulator, phase locked loop, LC-voltage controlled oscillator, phase frequency detector, charge-pump, phase generator, phase selection, fractional spurs, phase-noise, fractional division.

To my dear mother, Azza Abu Gabal With all my love and gratitude

ACKNOWLEDGEMENT

First of all, thanks God for giving me the ability to finish this work. I am always helpless without your support.

I would like to express my deep gratitude to Dr. Mohamed El Nozahi for his continuous help, supervision and support. He is the one who taught me to be a researcher. He taught me how to start a research, how to start a design, how to analyze problems and track errors in order to find a solution to the problem. He taught me how to present my work. He even taught me how to be persistent, patient and accurate. Dr. Mohamed, I owe you a lot.

Many thanks to Prof. Adel El Hennawy for his great help and support. I got great benefit from him since my pre-master courses. He always has a great ability in illustrating scientific materials. Many thanks to Prof. Hassan El Ghitany who was the one who taught me the basics of electronics since I was an undergraduate student. He was also the one who advised me to make my research in fractional-N frequency synthesizers.

I would like to thank all the teaching staff in Electronics and Communications department, ASU, who taught me to be an engineer, to be able to think correctly and to survive hard times. Special thanks to Prof. Hani Fekri, Dr.Wael Fekri, Dr. Emad Hegazi, Dr.Khaled Sharaf, Prof. Safwat Mahrous and Prof. Salwa el Ramly. Many thanks to eng. Bichoy Wageih and eng. Joseph Riad for their great help and patience.

I would like to express my deep gratitude to my parents, my dear dad who has been struggling since the moment of my birth till now for my sake, and my dear mum with her continuous support at every moment of my life, making lots of effort and sacrificing her whole life for the sake of my comfort, prosperity and happiness. She has always been my guiding angel, pushing me to be in the front lines in all fields since I was a little girl.

I would also like to express my deep gratitude to my beloved husband Khaled Samir who has been a real support for me throughout this work. Without his understanding and encouraging, it would have been very difficult for me to finish this work. Really, thanks Khaled for making things that simple for me, thanks for being that broadminded man in my life.

My dear sisters, Aya and Lobna, many thanks for your unconditional help and support. My beautiful daughter Farida, thanks for being my motive to finish this work. My close friend Nehad Mansour, thanks for your continuous help and support by all means. My dear parents in law, thanks for your encouragement, support, help and care throughout this work.

CONTENTS

LIST OF FIGURES	V
LIST OF TABLES	X
LIST OF ABBREVIATIONS	xi
LIST OF SYMBOLS	xii
CHAPTER 1: INTRODUCTION	1
CHAPTER 2: BASICS OF FREQUENCY SYNTHESIZERS	
2.1 Definition.	3
2.2 PLL Basics	3
2.3 PLL Building Blocks.	7
2.3.1 Phase Detector	7
2.3.2 Charge Pump.	11
2.3.3 Loop Filter	13
2.3.4 Voltage Controlled Oscillator.	15
2.3.5 Frequency Dividers	21
2.3.5.1 Integer-N Frequency Dividers	21
2.3.5.2 Fractional-N Frequency Dividers	23
2.4 Performance Metrics.	27
2.4.1 Tuning Range	27
2.4.2 Frequency Resolution.	27
2.4.3 Frequency Accuracy	28
2.4.4 Phase Noise	28

2.4.5 Spurious Signals
2.4.6 Settling Time
2.5 Noise in Frequency Synthesizers
2.6 Fractional-N Frequency Synthesizers State-of-the-Art Survey35
2.6.1 Architectures
2.7 Conclusion
CHAPTER 3: FRACTIONAL DIVISION USING PHASE SELECTION
3.1 Introduction
3.2 Fractional Division
3.3 The main idea of the thesis
3.4 The Architecture
3.5 Blocks used to implement the idea
3.5.1 The Phase Generator
3.5.2 Delta-Sigma phase selection block
3.5.3 The 16 to 1 Multiplexer
3.6 Mathematical calculation of fractional spurs
3.7 Phase-switching $\Delta \Sigma$ fractional-N frequency synthesizers versus conventional frequency synthesizers
3.8 conclusion69
CHAPTER 4: PHASE-SWITCHING DELTA-SIGMA FRACTIONAL-N FREQUENCY SYNTHESIZER FOR LTE TRANSCEIVER
4.1 Introduction to LTE

	4.2 LTE specifications	70
	4.3 Top-level PLL description.	71
	4.4 System-level design steps for LTE integer-N frequency synthesizer	72
	4.5 Verifying the functionality of the designed integer-N frequency synthesizer	80
synthesiz	4.6 Verifying the functionality of LTE phase-switching Δ∑ fractional-N frequencer	-
	4.7 Conclusion	86
	ER 5: TRANSISTOR- LEVEL DESIGN OF THE LTE PHASE SWITCHING IONAL-N FREQUENCY SYNTHESIZER	GΔ
	5.1 Introduction.	87
	5.2 Phase-Frequency Detector Design.	88
	5.3 Charge-Pump Design.	93
	5.4 Voltage Controlled Oscillator Design.	100
	5.5 Phase Generation Block Design.	11
	5.6 Multiplexer Design	.118
	5.7 Divider Design.	121
		100
	5.7.1 2/3 Prescaler Design.	.123
	5.7.1 2/3 Prescaler Design	
		.127
	5.7.2 Swallow Counter Design.	.127 128

REFERENCES	
APPENDIX	137

LIST OF FIGURES

Figure 2.1 Basic PLL block diagram	4
Figure 2.2 Basic PLL linear model	5
Figure 2.3 XOR Phase Detector Characteristic	7
Figure 2.4 PFD based on D-flip flops.	8
Figure 2.5 PFD transfer function.	8
Figure 2.6 The operation of the PFD.	9
Figure 2.7 Pulses used for dead-zone removal.	10
Figure 2.8 Cycle slipping	11
Figure 2.9 CP placed after the PFD	12
Figure 2.10 2 nd order loop filter	13
Figure 2.11 Transfer characteristics of VCO	15
Figure 2.12 LC oscillator and ring oscillator	16
Figure 2.13 LC based oscillator.	18
Figure 2.14 VCO modes of operation.	19
Figure 2.15 A divide-by-6 counter	21
Figure 2.16 A pulse swallow frequency divider	22
Figure 2.17 Using an accumulator to perform dithering operation	23
Figure 2.18 Fractional division using an accumulator	24
Figure 2.19 Phase error when carrying out fractional division using accumulators	25
Figure 2.20 Using phase interpolation technique	26
Figure 2.21 The output spectrum of a frequency synthesizer	28
Figure 2.22 The effect of noisy oscillator used in the receiver	29
Figure 2.23 A linear model for PLL illustrating all noise sources	3
Figure 2.24 DLL phase poise	3/

Figure 2.25 Phase-noise of Delta-Sigma PLL.	35
Figure 2.26 A noise filter architecture	36
Figure 2.27 A dual loop architecture	37
Figure 2.28 An architecture with a loop bandwidth of 2 MHz.	38
Figure 2.29 A quantization-noise suppression technique	38
Figure 2.30 An architecture to lower the supply voltage for high frequency operation	39
Figure 3.1 Phase switching Delta-Sigma fractional-N frequency synthesizer	45
Figure 3.2 An illustration of the idea of phase selection.	47
Figure 3.3 Delta-Sigma phase selection block.	48
Figure 3.4 MASH 1-1-1 Delta-Sigma modulator block diagram	49
Figure 3.5 Illustration of the new idea used to carry out fractional division using a flow char	t57
Figure 3.6 A square wave with variable duty cycle	60
Figure 3.7 M(s) representation.	61
Figure 3.8 M(s) shifted by f ₁	62
Figure 3.9 M(s) shifted by f ₂	62
Figure 3.10 The modulating signal m(t) in case of dividing by 1/32	62
Figure 3.11 VCO output spectrum in case of having a fractional division ratio = 1/32	63
Figure 3.12 The modulating signal to get a division ratio of 1/32 using a simplified version of new idea	of the 64
Figure 3.13 The VCO output spectrum when a fractional division ratio of 1/32 is achieved us the simplified version of the new idea.	
Figure 3.14 Phase-switching $\Delta \Sigma$ fractional-N frequency synthesizer	66
Figure 3.15 Conventional fractional-N frequency synthesizer.	67
Figure 3.16 The output frequency spectrum in case of using the phase-switching $\Delta \Sigma$ fraction frequency synthesizer	
Figure 3.17 The output frequency spectrum in case of using the conventional fractional-N frequency synthesizer	68
Figure 4.1 Phase-switching Delta-Sigma fractional-N frequency synthesizer	71

Figure 4.2 Integer-N PLL	72
Figure 4.3 1 st order loop filter	73
Figure 4.4 The 2 nd order loop filter	75
Figure 4.5 The relation between C_1/C_2 and the phase margin	76
Figure 4.6 3 rd order loop filter	78
Figure 4.7 The settling behavior of the designed integer-N frequency synthesizer	80
Figure 4.8 VCO output at N = 260	81
Figure 4.9 VCO output at N = 190	81
Figure 4.10 Frequency spectrum of the designed integer-N frequency synthesizer	82
Figure 4.11 Phase-switching Delta-Sigma fractional-N frequency synthesizer	83
Figure 4.12 Settling response to 2.001GHz.	84
Figure 4.13 The VCO output at N = 200.1	84
Figure 4.14 Frequency spectrum of the designed fractional-N frequency synthesizer at 1	F=1085
Figure 5.1 Phase switching Delta-Sigma fractional-N frequency synthesizer	87
Figure 5.2 Phase-Frequency Detector (PFD)	88
Figure 5.3 PFD time response when the reference signal leads the output signal of the company of	
Figure 5.4 PFD time response when the reference signal lags the output signal of the di 30ns.	
Figure 5.5 PFD time response in lock state	90
Figure 5.6 Zoomed view at the falling edges of the inputs	91
Figure 5.7 PFD phase-noise.	92
Figure 5.8 CP schematic	93
Figure 5.9 The output of the charge pump when the upper part of the CP is on	96
Figure 5.10 The output of the charge pump when the lower part of the CP is on	97
Figure 5.11 Variation of Icp in response to variation in the output voltage (when the up on)	

Figure 5.12 Variation of Icp in response to variation in the output voltage (when the lon)	
Figure 5.13 Charge-pump phase-noise	99
Figure 5.14 Phase-noise produced from both PFD and CP	99
Figure 5.15 VCO Schematic	100
Figure 5.16 Important relations in choosing L	101
Figure 5.17 Capacitor array used for tuning VCO.	104
Figure 5.18 Tuning curve of VCO showing the effect of digital control of switches	105
Figure 5.19 The VCO output at a synthesized frequency of 1.9GHz	107
Figure 5.20 The VCO output at a synthesized frequency of 2.6GHz	108
Figure 5.21 VCO phase-noise at a synthesized frequency of 1.9GHz	108
Figure 5.22 VCO phase-noise at a synthesized frequency of 2.6GHz	109
Figure 5.23 Level shifter schematic	110
Figure 5.24 Phase generator block diagram.	111
Figure 5.25 D-flip flop using CML	112
Figure 5.26 D flip-flop.	113
Figure 5.27 Eight output waves of the phase generator showing that 45° phase is achieved the phase generator showing that 45° phase is achieved the phase generator showing that 45° phase is achieved the phase generator showing that 45° phase is achieved the phase generator showing that 45° phase is achieved the phase generator showing that 45° phase is achieved the phase generator showing that 45° phase is achieved the phase generator showing that 45° phase is achieved the phase generator showing that 45° phase is achieved the phase generator showing that 45° phase is achieved the phase generator showing that 45° phase is achieved the phase generator showing the pha	eved115
Figure 5.28 The phase pattern produced in case of a phase difference of 45 degrees befirst and fifth waves.	
Figure 5.29 The phase pattern produced in case of a phase difference of 225 degrees first and fifth waves	
Figure 5.30 simple differential amplifier used for buffering the VCO output	117
Figure 5.31 The schematic of the multiplexer used	119
Figure 5.32 Phase difference detection schematic.	120
Figure 5.33 Pulse swallow divider.	121
Figure 5.34 The operation of the pulse swallow divider at $S = 1$	122
Figure 5.35 The operation of the pulse swallow divider at $S = 19$	122

Figure 5.36 2/3 Prescaler	123
Figure 5.37 D flip-flop used in the dual modulus prescaler.	124
Figure 5.38 The divide-by-2 operation performed by the prescaler.	126
Figure 5.39 The divide-by-3 operation performed by the prescaler.	126
Figure 5.40 the swallow counter block diagram.	127
Figure 5.41 JK flip-flop used in the swallow counter.	128
Figure 5.42 Program counter block diagram.	129
Figure 5.43 The operation of a divide by 23 program counter	129
Figure 5.44 The settling behavior of the loop when the output frequency is 2.6GHz	130