**AIN SHAMS UNIVERSITY**
**FACULTY OF ENGINEERING**
**CAIRO-EGYPT**
Electronics and Communications Engineering Department

# Designing outer channel codec for DVB-T

A dissertation
Submitted in Partial Fulfillment for the Requirements of the Degree of
Master of Science in Electronics and Communications Engineering

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# STATEMENT

This dissertation is submitted to Ain-Shams University in partial fulfillment for degree of Master of Science in Electronics and Communication Engineering.

The work included in this dissertation was carried out by the author at the Electronics and Communications Engineering Department, Ain Shams University.

No part of this dissertation has been submitted for a degree or a qualification at any other university or institute.

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Signature: Sara Kamar Mohamed Mousa.

Date: 16 / 04 /2018.

*To My Father,*

*To My Mother,*

*To My Husband*

*& My Littles Sara & Omar*

*I present to you this dissertation.*

*May I by this express my deepest gratitude and love*

***Thanks***

*Without you, I could not have reached this successful step in my life*

# Abstract

**Sara Kamar Mohamed**

**Designing outer channel codec for DVB-T**

**Master of Science dissertation**
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Digital television (DTV) provides a huge amount of information to many users at low cost. Recently, it can be packaged and fully integrated into completely digital transmission networks. Reed-Solomon codes (RS) is one type of error correcting codes that can be used to enhance the performance of DTV. Interleaving/deinterleaving process enhances the performance of channel errors by spreading out random errors, very high-speed hardware description language (VHDL) is used in electronic design automation. It can be used as a general purpose parallel programming language.

This Thesis presents VHDL program for Reed-Solomon codec (204,188) and convolutional interleaver/deinterleaver, used in Digital Video Broadcasting-terrestrial system (DVB-T), according to ETSI EN 300 744 V1.5.1 standard. The VHDL programs are implemented on Xilinx 12.3 ISE and then simulated and tested via ISE simulator then the code is synthesized on FPGA device the results are compared with IP core for Xilinx 12.3 ISE which gives the same results.

**Key words:** Convolutional interleaver/deinterleaver, DVB-T, outer coding, RS (204,188), VHDL.

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# Dedication

*I would like to dedicate this dissertation to my father* ***Kamar Mousa****, my mother* ***Kolthom EL-Attar*** *and my husband,* ***Eng. Ahmad Fath-Allah****, who have been an inspiration throughout my life and who have been supportive for all I have achieved. I wish dedicate this dissertation to my sisters, my brothers, my daughter* ***Sara****, my son* ***Omar*** *and my mother in law for their support and encouragement.*

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