بسم الله الرحمن الرحيم

شبكة المعلومـــــات الجامعية

التوثيق الالكتروني والميكروفيلم

شبكة المعلومات الجامعية

جامعة عين شمس

التوثيق الالكتروني والميكروفيلم

﴿ قـــســـم ﴾

نقسم بالله العظيم أن المادة التي تم توثيقها وتسجيلها
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لم ترد بالأصـــل

Cairo University
Faculty of Engineering

FPGA Implementation of CAN (Controller Area Network) Protocol

By

Mohamed Khaled Ibrahim AL-Mekkawy

A thesis Submitted to the
Faculty of Engineering at Cairo University
In partial fulfillment of
Requirements for the Degree of
MASTER OF SCIENCE
In Electronics and Communications Engineering

Supervised by

Prof. Dr. Aly Ezzat Salama
Electronics & Communications Department.
Faculty of Engineering.
Cairo University.

Faculty of Engineering, Cairo University,
Giza, Egypt
July 2006

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Abstract

The CAN (Controller Area Network) communication serial protocol is a carrier-sense multiple access protocol with collision detection and arbitration on message priority (CSMA/CD+AMP) with a multi-master serial communication bus using twisted pair cables as transmission medium. It suites applications require high number of short messages for multi recipients. System-wide data consistency is mandatory in a short period of time with high reliability in rugged operating environments. The CAN protocol is well adapted for real-time controls applications due to its predictable medium access approach with the collision avoidance, hierarchically identifier message and multiple errors detection features.

In this thesis we present a design and implementation of CAN protocol by algorithm, which deploys majority voting technique for accurate synchronization that suites military and space applications. We had studied carefully the CAN protocol with all its cases and its implementations in the market. The design had been tested with all the possible normal and error cases and we also studied carefully the Synchronization techniques available and choose the proper way of synchronization to comply the design taking into consideration hardware and software synchronization. CAN-FPGA supports CAN A (11 bit identifier) and B (extended format with 29 bit identifier). The data handling between the FPGA and the host controller is through the eight-bit wide data bus and the addressing is through the five-bit address bus. Our FPGA supports the overload frame and able to detect all types of errors stated in the standard. CAN-FPGA supports the retrieving of messages from the CAN controller receive buffer areas before they are overwritten by further incoming messages by notifying the host controller in case of full and empty the receiving register through certain signal indication. The design has been implemented on Actel and Xilinx FPGAs using Actel Libero and Xilinx ISE respectively with a comparison to actual commercial designs in the market. The simulation results of some critical case studies on FPGA are demonstrated to prove the efficiency of the design on the level of software and hardware.

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