Ain Shams University
Faculty of Engineering
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Custom Layout in Deep Sub-Micron Processes

A thesis
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AIN SHAMS UNIVERSITY
FACULTY OF ENGINEERING
Electronics Engineering and Electrical Communications

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Statement

This dissertation is submitted to Ain Shams University for the degree of Master of Science in Electrical Engineering (Electronics and Communications Engineering).

The work included in this thesis was carried out by the author at the Electronics and Communications Engineering Department, Faculty of Engineering, Ain Shams University, Cairo, Egypt.

No part of this thesis was submitted for a degree or a qualification at any other university or institution.

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Custom Layout in Deep Sub-Micron Processes

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Masters of Science Dissertation
Electronics and Communications Department
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ABSTRACT

In recent years, the Systems-On-Chip advanced in technology and complexity to support the contentiously added modules and functionalities required to be implemented on a single chip. Although, most of the functions are implemented with digital circuitry, the interface with the real world makes an analog part a necessity. In terms of chip area, the analog part of the circuitry is usually not the major contributor, but still the one requiring most of the effort and time for closure. The progress in digital design CAD tools enabled digital design engineers to accommodate the increased size and functionality of digital circuitry, while on the other hand the design automation capabilities of analog CAD tools did not increase equally. Different analog design automation approaches have been attempted; however, no generic automation methodology can be followed as the problem is less systematic and encompasses many trade-offs.

From process technology perspective, as the technology scales down towards the sub-micron processes new Layout Dependent Effects (LDE) are introduced. These effects are layout dependent, hence can't be accurately taken into consideration until the layout phase of the design is started. To achieve post-layout successful designs that meet all the specifications, typically many iterative loops between the schematic and physical design are required.

This thesis provides an overview on the analog layout placement challenges in deep sub-micron processes. A custom layout automated placement flow is introduced using Satifiability Modulo Theories (SMT). The goal is to find the feasible placements for the building blocks construing the design top-level which meet the assigned area and aspect ratio. Also, a stress-aware device pattern generation flow is introduced which allows the

designer to estimate and take into consideration the layout stress degradation effect early in the device pattern generation phase. Finally, real design examples are used to demonstrate the proposed flow, and a discussion on the obtained results is presented.

Key words: Analog, Layout, Placement, Automation, SMT, Shape Function, Aspect Ratio, LDE, Stress-Aware, STI.

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