AINSHAMS UNIVERSITY
FACULTY OF ENGINEERING
CAIRO - EGYPT

CMOS LTE Receiver Front-End

A Thesis

Submitted in partial fulfillment for the requirements of the degree of
Master of Science in Electrical Engineering

Submitted by

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STATEMENT

This thesis is submitted to Ain Shams University in partial fulfillment of the degree of Master of Science in Electrical Engineering.

The work included in this thesis was carried out by the author in the Department of Electronics and Communications Engineering, Ain Shams University.

No part of this thesis has been submitted for a degree or a qualification at any other university or institute.

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DEDICATION

To my parents and my beloved husband, for their everlasting love and support.

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Published Papers

[1] "Wideband Inductorless CMOS RF Front-End For LTE Receivers", accepted on IEEE, ICICDT conference, Texas, USA, May. 2017

CMOS LTE Receiver Front-End

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Abstract

More recent, Long Term Evolution (LTE) has been broadly contemplated. The third generation partnership project (3GPP) proposes a Universal Mobile Telephone System (UMTS) which studies several alternative technologies before choosing Wideband Code Division Multiple Accesses (W-CDMA) for the radio access network. The continuing improvements in radio frequency (RF) front-end technology have led to many new and fascinating applications in the fourth generation (4G) wireless communications. The LTE standard takes advantage of the multi-carrier modulation scheme Orthogonal Frequency-Division Multiplexing (OFDM) to increase spectral efficiency, which demands higher linearity because of a non-constant signal envelope. LTE supports both Frequency- Division Duplex (FDD) and Time Division Duplex (TDD) with the wide range of frequency bands from 0.7 GHz to 2.7 GHz in addition to a wide number of channel bandwidth that allocated from 1.4 MHz to 20 MHz.

The use of Complementary Metal Oxide Semiconductor (CMOS) technology in the RF front-end for LTE has increasingly been the object of study over the past few years due to their low power consumption and small physical size. With the increasing usage of mixed-signal integration, reliability requirements for analog CMOS circuit applications have become more critical. The final goal in CMOS integration is to create a monolithic wireless receiver that covers whole RF front-end and baseband. Thus, CMOS process is a suitable candidate for LTE RF front-end development for integration with the digital part.

Different techniques have been proposed for LTE transceiver implementation. In this thesis, the design and implementation of a single path wide band frequency front-end receiver have been presented by using UMC 0.13μm CMOS technology. The LTE receiver covers 0.7 GHz to 2.7 GHz.

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The proposed design reduces the system complexity and opens the opportunity to increase the integration level and lower power consumption, despite its simplicity. The key building design blocks for the proposed LTE receiver are microstrip patch antenna, wide band active balun, low noise amplifier (LNA) and mixer.

The first part of the thesis is to design the passive part of LTE receiver by designing a microstrip patch antenna with defected ground structure. The proposed antenna is fabricated using FR-4 material substrate with dielectric constant of ε_r =4.4, height h_{sub}= 1.6 mm and loss tangent δ = 0.02. The overall dimensions of the antenna are 10mm x10mm x1.6mm with 50 Ω impedance. The antenna operates between 0.7G Hz to 3GHz for return loss -6 dB. The simulated antenna achieved a bout average radiation efficiency of 80 %, average antenna gain of about 4.2 dB with omnidirectional radiation pattern over the operating band. The proposed antenna was fabricated using the photolithographic method and measured using the vector network analyzer N9918A. There are good agreements between the simulated and measured results. All simulations are carried out using 3D EM commercial High Frequency Structural Simulator (HFSS) ver. 14.0.

The second part is to design the active part of the front end receiver which includes balun, low noise amplifier, and mixer. Optimization of current reuse LNA using linearization technique followed by NMOS switches mixer stage are effectively used to achieve maximum gain, low noise figure, and low power consumption The circuit level simulation will be carried out using ADS tool, while layout design and verification will be obtained by cadence tool. Each component was simulated separately and then the three components were combined with the fabricated antenna to make a RF front-end for LTE applications. At the pre-simulation, the receiver front-end provides a reasonable balun matching with an S_{11} below -10 dB and S_{21} ranges from 15 to 22 dB. The in band IIP3 ranges from -3 dBm to -9.8 dBm and NF ranges from 7.5 dB to 5.6 dB while the power consumption is 26.14 mW. At post-simulation, the receiver front-end provides a reasonable balun matching with an S_{11} below -9 dB and S_{21} ranges from 15 to 20 dB. The in band IIP3 ranges from -4 dBm to -10.2 dBm and NF ranges from 7.9 dB to 6.5 dB while the Power consumption 26.14 mW from a 1.2 V supply. Using these optimizations, our proposed receiver can be a good candidate for LTE applications**.** The layout of the design occupies 0.362 mm^2

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