ASYNCHRONOUS SAR-ASSISTED TWO-STAGE PIPELINE ANALOG TO DIGITAL CONVERTER USING RING AMPLIFIER

By

Karim Moataz Mohamed Mahmoud Ali Megawer

A Thesis Submitted to the
Faculty of Engineering at Cairo University
in Partial Fulfillment of the
Requirements for the Degree of
MASTER OF SCIENCE
in
ELECTRONICS AND COMMUNICATIONS ENGINEERING

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Title of Thesis:

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Key Words:
Analog to Digital Converter; Pipeline ADC; SAR ADC; Ring Amplifier.

Summary:
In this thesis, an adaptive ring amplifier is proposed to introduce a degree of freedom in speed/stabilization design trade-off in the original ring amplifier. It also introduces an area efficient solution for the auto-zeroing stability problem that the conventional ring amplifier suffers from. The proposed adaptive ring amplifier improves the linearity by 10dB at the same operating frequency. Moreover, it achieves a 40% improvement in the operating frequency for the same linearity and settling requirements. It has a 98% area reduction compared to the conventional ring amplifier for the same stability conditions. A 12-bit 25MS/s SAR-Assisted two-stage pipeline ADC is designed and implemented in a low-cost 0.13 μ m CMOS technology. It consists of a 6-bit first stage followed by a 7-bit second stage utilizing the proposed adaptive ring amplifier in order to meet the stringent specifications. In addition, a detect-and-skip (DAS) capacitive DAC (CDAC) switching method is used to reduce the switching energy of the first-stage CDAC. The ADC consumes 0.89mW achieving a Figure of Merit (FoM) of 13.7 fJ/conversion-step while operating from a single 1.2V supply.

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Table of Contents

List of Tables