Ain Shams University
Faculty of Engineering
Electronics and Communications Department

Layout Automation of Analog Integrated Circuits

A thesis
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FACULTY OF ENGINEERING
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Layout Automation of Analog Integrated Circuits

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Statement

This dissertation is submitted to Ain Shams University for the degree of
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The work included in this thesis was carried out by the author at the Electronics and Communications Engineering Department, Faculty of Engineering, Ain Shams University, Cairo, Egypt.

No part of this thesis was submitted for a degree or a qualification at any other university or institution.

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Layout Automation of Analog Integrated Circuits

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Masters of Science Dissertation
Electronics and Communications Department
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ABSTRACT

In recent years, Systems On Chip has advanced in technology the thing that has added more complexity to cope with where there are contentiously added blocks and functionalities that is required to be integrated in one chip. Most of the functions are implemented using digital circuitry, However the interface with the real world makes an analog part a necessity. In terms of chip area, the analog part of the circuitry is only almost 20% of the design, but still the most expensive part of the design process from the aspect of effort and time needed for closure. The progress in digital design Computer-Aidded-Design CAD tools has given the digital design engineers the flexibility to accommodate with the increased size and functionality demanded from the digital circuitry, on the other hand the analog part is still suffering from the shortage of (CAD) tools to help the designers out for completion of analog part with less effort and time. There have been different analog design automation approaches attempted but, still no generic automation methodology can be adopted as the problem is much less systematic and has many variability that must be accounted for.

Retargeting has been adopted to take advantage of the new technologies benefits that is continuously progressing and serving the continuous advancing needed requirements, where the qualified analog circuits that has passed post fabrication testing and silicon proven are re-used with advanced technologies. This thesis presents an efficient methodology for automatic analog layout process retargeting, which fits in the current design flow. It relies on two concepts: First, the reuse of source layout heuristics and matching considerations through device placement constraint extraction. This allows an automatic layout reconstruction using foundry Parametric Cells (PCells) of the target process, as in the current

design flow. Second, feeding those constraints to an analog layout automatic placer based on Satisfiability Modulo Theories (SMT). Besides conserving the source layout topology, this also allows generating multiple layout options in case of large changes of device dimensions and/or requiring a new aspect ratio in the target process. Two test cases of a Miller-OTA and a two-stage comparator demonstrate the proposed flow.

Key words: Analog Layout, Placement, Automation, SMT, Retargeting.

Summary

This thesis discusses an overview on the analog layout design challenges in deep sub-micron processes and the impact of time and effort needed to accomplish retargeted analog circuit. State of the art in analog layout placement retargeting automation flows is presented, as well as an automated analog layout placement retargeting flow based on Satisfiability Modulo Theories (SMT) are proposed. Finally, real design examples are used to demonstrate the flow proposal.

This thesis is divided into five chapters including lists of contents, tables and figures as well as list of references and one appendix:

Chapter 1

This chapter provides an overview on the analog layout retargeting challenges. Motivation, objective and contributions of this work are illustrated. Also, the organization of the thesis is highlighted.

Chapter 2

This chapter discusses the analog design flow as well as analog design retargeting. State of the art is discussed and finally the SMT based analog placer that has been employed in this work has been discussed.

Chapter 3

An analog layout retargeting placement flow based on Satisfiability Modulo Theories analog placer is proposed. The flow considerations, a step by step introduction to the proposed flow and the flow architecture are discussed.

Chapter 4

This chapter provides a demonstration of layout placements obtained for the two real designs examples using the proposed flow. The results and final achieved layouts are shown as well as comparison to previous flows performance. Finally, a discussion on the results and highlights on the benefits of the proposed flow are discussed.

Chapter 5

This chapter concludes the work presented in this thesis, and highlights the proposed future work.

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