Ain Shams University
Faculty of Engineering
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Ultra Low Power CMOS Front-End for Medical Implants

A Thesis

Submitted in partial fulfillment for the requirements of Master of Science degree in Electrical Engineering

Submitted by:

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بسم الله الرحمن الرحيم

(وَمَا أُوتِيتُمْ مِنْ الْعِلْمِ إِلاَّ قَلِيلاً)

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Statement

This dissertation is submitted to Ain Shams University for the degree of Master of Science in Electrical Engineering (Electronics and Communications Engineering).

The work included in this thesis was carried out by the author at the Electronics and Communications Engineering Department, Faculty of Engineering, Ain Shams University, Cairo, Egypt.

No part of this thesis was submitted for a degree or a qualification at any other university or institution.

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Abstract

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This thesis presents low-voltage, low-power, low-noise system and circuit design techniques of bio-medical front-ends. The target application is a compact and digitally-programmable neural front-end to be used in brain machine interface (BMI) systems with large number of channels in deep sub-micron CMOS technologies.

On the system level, a new mixed-signal architecture is proposed to minimize area of the neural front-end to be used with the emerging multi-channel BMI systems. The conventional electrode offset suppression technique is analog high-pass filtering using large input coupling capacitors, which consume large area, and pseudo-resistors, which varies significantly with process, voltage, and temperature (PVT) variations. The proposed front-end employs a single multi-bit $\Sigma\Delta$ digital-to-analog converter (DAC) with dynamic element matching (DEM) and a flexible digital filter in the feedback to suppress electrode DC offset up to $\pm$50 mV and digitally control the front-end closed loop transfer function. The flexible digital filters can be configured to acquire different neural signal: Local field potential (LFP) signals only, spikes signals only, or both.

On the circuit level, different analog and digital blocks in the neural front-end exploit low supply voltage of 0.8 V to minimize the power consumption and to make the neural front-end more compatible with emerging wireless powering schemes. This low supply voltage imposes limitation in the dynamic range. Thus, all analog blocks utilize fully differential circuit implementation. Furthermore, the usage of the mixed-signal feedback relaxes the requirements of the dynamic range as it desensitizes the overall gain of the neural front-end. Hence, an open-loop compact low-noise neural amplifier is used as the first block in the front-end. A second order Gm-C anti-aliasing filter is used to filter out $\Sigma\Delta$ DAC quantization noise. A 8-bit 800 kS/s SAR ADC is proposed with 48.5 SNDR and 11.3 fJ/conversion-step to be multiplexed by 4 channels.

A top down design methodology was adopted to implement the proposed mixed-signal front-end in a standard 0.13 μm CMOS technology. A complete frequency domain linear model is developed where the system performance is analyzed and optimized then specifications of different blocks are calculated. Moreover, a complete time-domain behavioral model is built using Matlab/Simulink to account for non-linearities and non-idealities of different blocks in the system. The whole

neural front-end achieves a low input-referred noise of 4.83 μV_{rms} for a signal bandwidth of 10 kHz using a compact and highly programmable architecture. It consumes 8.8 μW from 0.8 V supply while occupying 0.046 mm^2.

Key words: Neural recording, brain machine interface, instrumentation amplifiers, antialiasing, neural interface

Summary

Chapter 1 is an introduction to the thesis. An extensive literature survey to brain machine interface (BMI) systems is demonstrated including state-of-the-art applications, classification of neural bio-potential signals, and BMI architectures. A brief introduction for different integrated circuits (ICs) modules of BMI systems is presented.

Chapter 2 presents an extensive survey on recent architectures of neural front-ends for BMI systems. The performance of the state-of-the-art neural front-ends is summarized in this chapter. Moreover, it describes the system architecture of a new mixed-signal neural front-end, it also illustrates the system design methodology. Then, a frequency-domain linear model of the entire system is developed. Using this model, the system performance is analyzed and optimized. The contribution of different blocks in the overall input-referred noise is analyzed using frequency domain transfer functions.

Chapter 3 describes the design methodology and the detailed analysis of different circuit blocks employed in the system. The architecture of each block is selected to satisfy stringent requirements of low supply voltage operation, noise performance, power consumption, area, and other specifications.

Chapter 4 presents a complete time-domain behavioral model for the whole system is built using Matlab/Simulink. It accounts for non-linearities and non-idealities of different blocks in the system. The model facilitates system verification and enables system simulation with real and synthesized neural signals. The overall noise performance and dynamic range of the neural front-end is simulated using fast and accurate behavioral simulation. Then, the performance of the proposed neural-front is compared to state-of-the-art designs.

Chapter 5 demonstrates thesis conslusion. Strengths and weaknesses of the proposed solutions are discussed and some directions for future research are suggested.

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