Ain Shams University
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Design of High Performance Analog to Digital Converter in Deep Sub-micron COMS Process

A Thesis
Submitted in partial fulfilment for the requirements of Master of Science degree in Electrical Engineering

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Statements

This thesis is submitted to Ain Shams University in partial fulfillment of the requirements for the degree of Master of Science in Electrical Engineering.

The work included in the thesis was carried out by the author at the Electronics and Communication Engineering Department, Faculty of Engineering, Ain Shams University, Cairo, Egypt.

No part of this thesis has been submitted for a degree or a qualification at any other university or institute.

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Abstract

Design of High Performance Analog to Digital Converter in Deep Sub-micron COMS Process
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The continuous effort to improve the performance of analog-to-digital converters (ADC) has led the development of several precision techniques for ADCs. The primary objective of those precision techniques is to alleviate the accuracy constraints such as capacitor mismatch, charge injection, finite op amp DC gain and comparator offset. In the early years, the error correcting techniques like the ratio independent, reference refreshing, capacitor error-averaging, on-chip capacitor trimming and analog calibration were applied in the analog domain. The main drawback of these analog precision techniques is the complexity of circuit implementation. The digitally controlled self calibration and digital-domain calibration techniques were introduced to eliminate the disadvantage of the analog precision techniques but developed for successive approximation and flash type ADCs, respectively. Reduced feature size combined with lower power supply voltage are the key technology drivers resulting in reduced cost, higher speed and lower power consumption of digitally calibrated ADCs.

This thesis presents a 1.0-V 13-bit 205-MSample/s time-interleaved pipelined analog-to-digital converter (ADC) with a 95-dB spurious free dynamic range (SFDR), 75.5-dB signal-to-noise-plus-distortion ratio (SNDR) over the full Nyquist band and a total power consumption of 71mW. This performance is enabled by digital background calibration of both capacitor mismatch in the multi-bit DAC and finite inter-stage gain errors. M-sequence characteristics was used for the generation of the multiple orthogonal codes needed in the calibration engine. Also, a simple design for the dithered re-quantizer which precedes calibration is adopted. Digital calibration achieves an improvement of better than 23-dB in SFDR and 13-dB in SNDR.

Key Words: ADC, CMOS, Time-interleaved, Pipeline, Low-Power, Calibration.

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