Delta Sigma Analog to Digital Converter for Video Applications

A Thesis

Submitted in partial fulfillment for the requirements of Master of Science degree in Electrical Engineering

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STATEMENT

This dissertation is submitted to Ain Shams University for the degree of Master of Science in Electrical Engineering, Electronics and Communications Engineering.

The work included in this thesis was carried out by the author at the Electronics and Communications Engineering Department, Faculty of Engineering, Ain Shams University.

No part of this thesis was submitted for a degree or a qualification at any other university or institution.

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M.Sc. Thesis

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ABSTRACT

Sigma–Delta techniques have been widely used for low-bandwidth and high-resolution applications owing to the oversampling and noise shaping feature. However, Sigma-Delta applications are being extended to new telecommunication areas, which typically require MHz range signal bandwidth with a higher sampling clock. The CMOS implementation of modulators is problematic due to the high-frequency limitations of the opamps and sampling switches. Time-interleaved (TI) modulators are an attractive solution for high-speed applications, since the oversampling rate (OSR) can be increased without speeding up the analog blocks.

In this thesis, a switched-capacitor circuit of a four-branched time-interleaved delta-sigma structure is presented. The circuit can be easily extended to M-branch modulator. In addition, double sampling was also used to increase time efficiency to its maximum. Both techniques together give the designer the extra freedom to trade-off circuit speed with die area.

SUMMARY

Although real world signals are analog, it is often desirable to convert them into the digital domain using an analog to digital converter (ADC). One of the motivating factors of this conversion is the high efficiency of transmission and storage of digital signals. One technique that has become quite popular for achieving A/D conversion with high resolution is sigma-delta modulation.

In this thesis, the design procedure -at macro model level- for the realization of time-interleaved oversampling converters is presented. Using the concept of block digital filtering technique to convert any arbitrary Sigma-Delta topology into corresponding time-interleaved structures. Combining the time-interleaved structure with double sampling to extend the effective sampling frequency in switched-capacitor Sigma-Delta modulators.

A Second-order four branches Sigma-Delta modulator is first presented. The switched-capacitor circuit is then constructed using double sampling techniques. Results show that the effective OSR is enhanced by a factor of 8 at the expense of larger area.

List of Symbols

A/D	Analog to Digital
ADC	Analog to Digital Converter
Cs	Sampling Capacitor
D/A	Digital to Analog
DAC	Digital to Analog Converter
DR	Dynamic Range (dB)
FFT	Fast Fourier Transform
Fm	Signal Bandwidth
Fs	Sampling frequency
K	Boltzmann constant
LSB	Least Significant bits
N	Number of Digital bits
n	Order of Sigma Delta modulator
Nsw	Switch Noise
OSR	Oversampling Ratio
Pin	Power of Input signal
PQ	Quantization noise power
SNR	Signal to Noise Ratio
T	Temperature
TI	Time interleaved
TIM	Time interleaved Modulation
X(n)	Input Samples
Y(n)	Output Samples

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Introduction

The emergence of powerful digital signal processors implemented in CMOS VLSI technology creates the need for high-resolution analog-to-digital (A/D) converters that can be integrated in fabrication technologies optimized for digital circuits and systems. However, the same scaling of VLSI technology that makes possible the continuing dramatic improvements in digital signal processor performance also severely constrains the dynamic range available for implementing the interfaces between the digital and analog representation of signals. A/D converters based on sigma-delta (A/D) modulation combine sampling at rates well above the Nyquist rate with negative feedback and digital filtering in order to exchange resolution in time for that in amplitude. Furthermore, these converters are especially insensitive to circuit imperfections and component mismatch since they employ only a simple two-level quantizer, and that quantizer is embedded within a feedback loop. Sigma-Delta modulators thus provide a mean of exploiting the enhanced density and speed of scaled digital VLSI circuits so as to avoid the difficulty of implementing. But the main drawback of Sigma-Delta modulators is their limitations in high bandwidth applications.

This thesis studies the most known Sigma-Delta techniques and try to use new technique named Time-interleaved modulating to overcome high bandwidth applications. In this techniques parallelism is exploited to relax the delta-sigma circuitry.

In Chapter 1, The basic theories that try to explain the Delta and Sigma-Delta functionality is proposed. Also the full derivation of basic parameters

have been produced. Finally the first and second order structures have been presented.

In Chapter2, The different design steps of second order sigma delta modulator have been studied. We started with the derivation of some extra parameters, then try to implement second-order sigma-delta modulator based on our experience from chapter 1. Finally, macro level model has been introduced for the whole system.

In Chapter 3, A complete survey of different Time Interleaved modulator techiques is introduced with special care of digital-block filter technique. Then full analysis of Optimized TIM techniques. Finally we introduce Two-path Sigma-Delta modulator.

In Chapter 4, Different efforts done to implement the optimized Time interleaved modulator at the macro level model. Second-order with 4 branches, doubled-sampled TIM sigma-Delta modulator. It is proved that the over sampling ratio is improved by factor of 8 , each branch contributes by factor of 2 due to double sampled techniques. Which in turns relax the modulator circuitry, but at the expense of circuit area.