



# **RESEARCH ON MEMRISTIVE- AND MEMCAPACITIVE-BASED GATE-LESS MEMORY ARRAYS**

By

**Ahmed Adel Mohamed Emara Kassem**

A Thesis Submitted to the  
Faculty of Engineering at Cairo University  
in Partial Fulfilment of the  
Requirements for the Degree of  
**MASTER OF SCIENCE**  
in  
**Electronics and Communications Engineering**

FACULTY OF ENGINEERING, CAIRO UNIVERSITY  
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**TITLE OF THESIS:**

**Research on Memristive- and Memcapacitive-based  
Gate-less Memory Arrays**

**Key Words:**

Memristor; Memcapacitor; Gate-less memory array; Sneak paths

**Summary:**

This work aims to explore the properties of emerging devices as memristors and memcapacitors. The use of these devices as memory cells in memory applications is investigated as well as the techniques used for information extraction. The work helps to better solve the problems of sneak paths in gate-less arrays, coupling capacitance between selection bars and non-uniformity of data distribution in the array. It also gives a guide to solving selection bar resistance effect for future work.

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# Dedication

To

*my parents:*

*Dr Adel*

and

*Dr Neamat,*

*my sister:*

*Ayah,*

and

*my brothers:*

*Abdel Rahman,*

and

*Ibrahim.*





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# List of Symbols and Abbreviations

Symbols	Description
$v$	Voltage.
$i$	Current.
$q$	Charge.
$\phi$	Magnetic flux.
$R$	Resistance.
$G$	Conductance.
$C$	Capacitance.
$L$	Inductance.
$t$	Time.
$M$	Memristance.
$W$	Memductance.
$R_{on}$	Low resistance state.
$R_{off}$	High resistance state.
$D$	Device width.
$w$	Doped region width.
$\mu_v$	Dopants mobility.
$\sigma$	Charge time integral.
$\rho$	Magnetic flux time integral.
$\alpha$	Device voltage order.
$\beta$	Device current order.
$\Xi$	Device complexity metric.
$Z$	Impedance.
$U$	Potential energy.
$F$	Force.