شبكة المعلومات الجامعية

بسم الله الرحمن الرحيم

شبكة المعلومات الجامعية

التوثيق الالكتروني والميكروفيلم

شبكة المعلومات الجامعية

جامعة عين شمس

التوثيق الالكتروني والميكروفيلم

قسم

نقسم بالله العظيم أن المادة التي تم توثيقها وتسجيلها
علي هذه الأفلام قد أعدت دون أية تغيرات

يجب أن

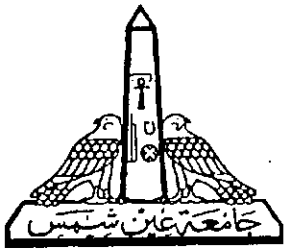
تحفظ هذه الأفلام بعيدا عن الغبار

في درجة حرارة من ١٥-٢٥ مئوية ورطوبة نسبية من ٢٠-٤٠%

To be Kept away from Dust in Dry Cool place of 15-25- c and relative humidity 20-40%

بعض الوثائـــــــق الاصليـــــة تالفـــة

بالرسالة صفحات لم ترد بالاصل



Ain Shams University
Faculty of Engineering
Computer and Systems Engineering Department

Combinational Equivalence Checking

A Thesis
Submitted in Partial Fulfillment of the
Requirements of the Degree of
Master of Science in Electrical Engineering
(Computer Engineering)

Submitted By

Sherief Mohamed Reda El-Edel

B.Sc. Electrical Engineering
(Computer & Systems Engineering)
Ain Shams University, 1998

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Statement

This dissertation is submitted to Ain Shams University for the degree of Master of Science in Electrical Engineering (Computer Engineering).

The work included in this thesis was carried out by the author at the Computer and Systems Engineering department, Faculty of Engineering, Ain Shams University.

No part of this thesis has been submitted for a degree or qualification at other university or institution.

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Abstract

Combinational Equivalence Checking

Sherief Mohamed Reda Ali El-Edel
Master of Science in Computer Engineering
Ain Shams University, 2000

Formal verification of digital circuits became an active research area in the last two decades. The pioneering work of Randal E. Bryant on Binary Decision Diagrams started a lot of research in this area. In addition, the shift of the design methodology from the schematic based to hardware description languages facilitates the introduction of formal verification in the design flow.

In this thesis, we focus on the combinational equivalence checking problem. We propose and implement three novel approaches. The first approach is based on reducing the search tree of the Boolean satisfiability formula using binary decision diagrams. The second approach integrates recursive learning and global implications in an iterative method. The third approach decomposes the circuits under verification and makes use of Boolean satisfiability, binary decision diagrams and functional learning to prove the circuit. In addition, we present a general verification framework where the different verification engines act as filters.

We also extend our work to sequential circuits. We study the reachability analysis problems of finite state machines. We show how don't cares can be used to reduce the transition relation BDD during symbolic image computation. We also perform reachability analysis using Boolean satisfiability and logic minimization techniques. Finally, sequential circuit verification based on the proposed techniques is studied and implemented.

For this thesis, the tool M-CHECK has been implemented in C for UNIX operating systems. The tool acts as a framework where the different ideas and algorithms are implemented and tested. The tool features 23 commands and it has been efficiently used to verify the ISCAS'85 benchmarks and industrial circuits of size up to 100K gates.

Keywords: Equivalence Checking, SAT, BDDs, Recursive Learning, Global Implications, Verification flow, ATPG, FSM symbolic traversal.

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