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Fast Locking Phased Locked Loop

A Thesis

Submitted in partial fulfillment for the requirements of the degree of Master of Science in
Electrical Engineering

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Mohamed Ali Ahmed

STATEMENT

This thesis is submitted to Ain-Shams University in partial fulfillment of the degree of Master of Science in Electrical Engineering.

The work included in this thesis was carried out by the author in the department of electronics and communications engineering, Ain Shams University.

No part of this thesis has been submitted for a degree or a qualification at any other university or institute.

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Abstract

Phase locked loop, PLL, is one of the most important synchronizing circuits used in many data transmission systems such as optical communications, telecommunications, disk drive systems, and local networks. A major characteristic of the PLL is the lock time; it is the time the PLL takes to adapt and settle after a sudden change of the input signal frequency. Conventional digital PLL (DPLL) can not satisfy the requirements of the high speed applications; it must be modified to achieve fast locking. Fast locking is required for fast frequency hopping among data bursts in high-speed digital communications. Fast locking is therefore a necessity for spread-spectrum communications, cellular phones, clock/data recovery circuits, etc. In this thesis, a DPLL is proposed to achieve fast locking by varying the PLL bandwidth. Wide bandwidth is used when the PLL is in the out-of-lock state, while the narrow bandwidth is used when the PLL is in the lock state. This can be accomplished by applying additional current to the conventional charge pump current in the out-of-lock state. The additional current is provided by a programmable charge pump (PCP). A frequency difference stage (FDS) is added to produce a 3-bit code represents the difference between the input and the output frequencies. This code is used to control the PCP output current. As the difference between the input and the output frequencies decreases, the PCP output current decreases to obtain smooth transition to lock. As locking is achieved, conventional CP current is used to provide loop stability. The proposed DPLL is designed using UMC 130nm CMOS process with a 1.2V power supply. It operates in the frequency range 100MHz – 1.5GHz. Over this frequency range, a locking time reduction up to 66% was achieved compared with conventional DPLL.

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List of Abbreviations

ADPLL: All Digital Phase Locked Loop.

APW: Adjustable Pulse Width.

CMOS: Complementary Metal Oxide Semiconductor.

CP: Charge Pump.

DAC: Digital to Analog Converter.

DAPD: Discriminator Aided Phase Detector.

DCO: Digital Controlled Oscillator.

DPLL: Digital Phase Locked Loop.

DSP: Digital Signal Processing.

FA: Full Adder.

FDS: Frequency Difference Stage.

FF: Flip Flop.

FM: Frequency Modulation.

HA: Half Adder.

LED: Light Emitted Diode.

LF: Loop Filter.

LPLL: Linear Phase Locked Loop.

OTA: Operational Transconductance Amplifier.

PCP: Programmable Charge Pump.

PD: Phase Detector.

PFD: Phase Frequency Detector.

PLL: Phase Locked Loop.

SPLL: Software Phase Locked Loop.

VCO: Voltage Controlled Oscillator.

List of Symbols

θ_e : Phase error signal.

K_d : PD gain.

u_d : PD output signal.

K_v : VCO gain.

ω_0 : VCO center frequency.

ω_2 : VCO output frequency.

u_f : LF output signal.

$\Delta\omega$: Frequency step.

N : Frequency division ratio.

$H(s)$: Closed loop phase transfer function.

θ_i : Input signal phase.

θ_o : Output signal phase.

$F(s)$: Loop filter transfer function.

$H_e(s)$: Phase error transfer function.

ω_n : Natural frequency.

ζ : Damping factor.

$\Delta\Phi$: Phase step.

$\Delta\omega_H$: Hold range.

$\Delta\omega_L$: Lock range.

$\Delta\omega_p$: Pull-in range.

T_L : PLL lock-in time.

$\Delta\omega_{po}$: Pull-out range.

I_{cp} : Charge pump current.

T_D : Delay time.

F_{in} : Input frequency.

F_{out} : Output frequency.

L : MOSFET channel length.

W : MOSFET channel width.

ω_p : Bandwidth.

φ_p : Phase margin.