AIN SHAMS UNIVERSITY
FACULITY OF ENGINEERING
CAIRO - EGYPT
Electronics and Communications Engineering Department

Fast Locking Phased Locked Loop

A Thesis
Submitted in partial fulfillment for the requirements of the degree of Master of Science in Electrical Engineering

Submitted by

Eng. Mohamed Ali Ahmed Ali

Electronics and Communications Eng. Dept.
Faculty of Engineering - Ain Shams University

Supervised by

Prof. Dr. Abdelhalim Abdelnaby Zekry

Communications and Electronics Department

Faculty of Engineering

Ain Shams University

Prof. Dr. Hamed Abdelghafar Elsimary

Head of Microelectronics Department

Electronics Research Institute

Cairo ٢٠١١

AIN SHAMS UNIVERSITY
FACULITY OF ENGINEERING
CAIRO - EGYPT

Examiners Committee

Name: **Mohamed Ali Ahmed Ali**

Thesis**: Fast Locking Phased Locked Loop**

Degree: **Master of Science in Electrical Engineering (Electronics and Communications Engineering)**

Title, Name and Affiliation	Signature
١- Prof. Dr. El Sayed Mostafa Saad	……..
Faculty of engineering, Helwan University	
٢- Prof. Dr. Adel Ezat Mohamed Elhenawy	……..
Faculty of engineering, Ain Shams University	
٣- Prof. Dr. Abdelhalim Abdelnaby Zekry	……..
Faculty of engineering, Ain Shams University	

Acknowledgments

All my thanks to Allah for the successful completion of this work. I express my deepest gratitude and thanks to **Prof. Dr. Abdel-halim A. Zekry**, Ain Shams University, for his continuous supervision support. Prof. Zekry is behind all analytical, technical and even spiritual actions throughout this work.

Also my deepest gratitude and thanks to **Prof. Dr. Hamed A. Elsimary**, Electronics Research Institute, for his understanding, patience, encouragement, besides, and overcoming any obstacles that might interfere with my work.

Also I would like to thank to Prof. Dr. Mahmoud Wagdy, California University, USA, for his useful notes on my work during his visits.

A special thanks to Dr. Heba A. Shawkey, Electronics Research Institute, for her great help and support along the way of my work.

Thanks to my friends Eng. Mohamed Gamal and Eng. Ghada Hamdy, Electronics Research Institute, for their technical support.

Many thanks for my mother, father, and brothers for their great hearts which looked after me all these years.

I am deeply grateful to my wife, who always encourages me for further progress.

Mohamed Ali Ahmed

STATEMENT

This thesis is submitted to Ain-Shams University in partial fulfillment of the degree of Master of Science in Electrical Engineering.

The work included in this thesis was carried out by the author in the department of electronics and communications engineering, Ain Shams University.

No part of this thesis has been submitted for a degree or a qualification at any other university or institute.

Name : Mohamed Ali Ahmed Ali

Signature:

Date : / /

Abstract

Phase locked loop, PLL, is one of the most important synchronizing circuits used in many data transmission systems such as optical communications, telecommunications, disk drive systems, and local networks. A major characteristic of the PLL is the lock time; it is the time the PLL takes to adapt and settle after a sudden change of the input signal frequency. Conventional digital PLL (DPLL) can not satisfy the requirements of the high speed applications; it must be modified to achieve fast locking. Fast locking is required for fast frequency hopping among data bursts in high-speed digital communications. Fast locking is therefore a necessity for spread-spectrum communications, cellular phones, clock/data recovery circuits, etc. In this thesis, a DPLL is proposed to achieve fast locking by varying the PLL bandwidth. Wide bandwidth is used when the PLL is in the out-of-lock state, while the narrow bandwidth is used when the PLL is in the lock state. This can be accomplished by applying additional current to the conventional charge pump current in the out-of-lock state. The additional current is provided by a programmable charge pump (PCP). A frequency difference stage (FDS) is added to produce a ٣-bit code represents the difference between the input and the output frequencies. This code is used to control the PCP output current. As the difference between the input and the output frequencies decreases, the PCP output current decreases to obtain smooth transition to lock. As locking is achieved, conventional CP current is used to provide loop stability. The proposed DPLL is designed using UMC ١٣٠nm CMOS process with a ١.٢V power supply. It operates in the frequency range ٢٥٠MHz – ١.٧٥GHz. Over this frequency range, a locking time reduction up to ٦٦% was achieved compared with conventional DPLL.

Table of Contents

List of Figures

List of Tables

List of Abbreviations

ADPLL: All Digital Phase Locked Loop.

APW: Adjustable Pulse Width.

CMOS: Complementary Metal Oxide Semiconductor.

CP: Charge Pump.

DAC: Digital to Analog Converter.

DAPD: Discriminator Aided Phase Detector.

DCO: Digital Controlled Oscillator.

DPLL: Digital Phase Locked Loop.

DSP: Digital Signal Processing.

FA: Full Adder.

FDS: Frequency Difference Stage.

FF: Flip Flop.

FM: Frequency Modulation.

HA: Half Adder.

LED: Light Emitted Diode.

LF: Loop Filter.

LPLL: Linear Phase Locked Loop.

OTA: Operational Transconductance Amplifier.

PCP: Programmable Charge Pump.

PD: Phase Detector.

PFD: Phase Frequency Detector.

PLL: Phase Locked Loop.

SPLL: Software Phase Locked Loop.

VCO: Voltage Controlled Oscillator.

List of Symbols

θ_e : Phase error signal.

K_d : PD gain.

u_d : PD output signal.

K_v: VCO gain.

ω_0 : VCO center frequency.

ω_2: VCO output frequency.

u_f: LF output signal.

$\Delta\omega$: Frequency step.

N: Frequency division ratio.

H(s): Closed loop phase transfer function.

Θ_i: Input signal phase.

Θ_o : Output signal phase.

F(s): Loop filter transfer function.

$\mathbf{H_e(s)}$: Phase error transfer function.

ω_n: Natural frequency.

ζ: Damping factor.

ΔΦ: Phase step.

Δw_H: Hold range.

Δw_L: Lock range.

Δwp: Pull-in range.

$\mathbf{T_L}$: PLL lock-in time.

Δw_{po}: Pull-out range.

I_{cp}: Charge pump current.

T_D: Delay time.

$\mathbf{F_{in}}$: Input frequency.

$\mathbf{F_{out}}$: Output frequency.

L: MOSFET channel length.

W: MOSFET channel width.

ω_p: Bandwidth.

φ_p: Phase margin.