IDENTIFYING WORST-CASE TEST VECTORS FOR LEAKAGE CURRENT AND DELAY FAILURES INDUCED BY TOTAL DOSE IN CMOS ASICS

By

Mostafa Mahmoud Abd El-Aziz Mohamed
Bachelor of Science in Computer Engineering
Cairo University

A Thesis Submitted to the
Faculty of Engineering at Cairo University
In Partial Fulfillment of the
Requirements for the Degree of
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Key Words:

Total Dose, ASIC, CMOS, Worst-Case, Test Vectors, Leakage Current, Logic failure, Delay failure.

Summary:

The test standard MIL-STD-883, method 1019, for testing electronic devices exposed to total-ionizing dose (TID) emphasizes the use of worst-case test-vectors (WCTV). However, they are typically not used in the total-dose testing of ASIC devices because they are known to be very difficult to identify. In the TID testing for space application, WCTV can be used to test the hardness assurance of a certain ASIC part before using it in space. This thesis discusses the development of novel methodologies which successfully identify, for the first time, the worst-case test-vectors for CMOS sequential ASIC devices targeting both leakage current failures, logic failures and delay failures induced by total-ionizing dose (TID). Those methodologies follow the typical design flow of ASIC device using standard-cell libraries. To identify the WCTV, we started by developing a cell-level fault model for each type of failure induced by total dose for all cells within a given standard-cell library. The fault models are implemented using a hardware descriptive language (HDL) and validated using SPICE simulations in where we use TID degraded MOS parameters. Next, we developed search algorithms to identify the WCTV of the ASIC devices. Finally, we verified our developed methodologies experimentally using a test chips (13 bit sequential bridge (for leakage and logic failures) and 8*8 combinational multiplier (for delay failures)) fabricated using ON Semiconductor 0.5 micron technology through MOSIS. The test chip was then exposed to gamma rays from Cobalt 60 (Co60) cell which produce 5K rad/minute. The measured results were consistent with those from our functional simulations of the ASIC devices using the developed fault models. Furthermore, the results show a significant difference between WCTV and other categories of test vectors.

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Dedication

This thesis is dedicated to my beloved wife who spent sleepless nights with and was always my support in the moments when there was no one to answer my queries. It is also dedicated to my father, who taught me that the best kind of knowledge to have is that which is learned for its own sake. It is also dedicated to my mother, who taught me that even the largest task can be accomplished if it is done one step at a time.

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Nomenclature

WCTV	Worst-Case Test-Vector
TID	Total Ionizing Dose
EM	Electromagnetic
DUT	Device under Test
HDL	Hardware Description Language
VHDL	Very High Speed Integrated Circuit (VHSIC) Hardware Description Language
ASIC	Application-Specific Integration Circuits
GA	Genetic Algorithms
ATPG	Automatic Test Pattern Generation
PSO	Particle Swarm Optimization

Abstract

The purpose of this thesis is to investigate the effects of radiation in CMOS ASICs circuits and develop a new methodology to identify worst case test vectors (WCTV) that induced leakage current and delay failures in these circuits.

In the past, the researchers studied the effect of radiation sources like x-ray and space on combinational and sequential circuits. They revealed that total ionizing dose caused the threshold voltage of MOS transistors to change because of trapping charges in the silicon dioxide gate insulator. For sub-micron devices these trapped charges can potentially "escape" by tunneling effects. Leakage currents are also generated at the edge of NMOS transistors and potentially between neighbor N-type diffusions. Commercial digital CMOS processes can normally stand a few radiation doses without a significant increase in power consumption. Modern sub-micron technologies tend to be more resistant to total dose effects than older ones. Furthermore, they identified a methodology to get WCTVs that induced logic failures and leakage current in combinational circuits.

For leakage current, the methodology starts by developing generic fault model which used to calculate leakage current that is induced in different CMOS cells like xor, aoi, or, …etc. then uses the genetic algorithm to find the WCTVs by generating random input vectors then calculate leakage current that is induced by these vectors using leakage current fault model.

For delay failures, the methodology begins by identifying fault model that calculates delay in different cells. Then the directed graph theory is used to select some critical paths. Finally the genetic algorithm is used to find the WCTVs for delay failures in selected critical paths using delay fault model.

The genetic algorithm is better than exhaustive search this is because exhaustive search examines a huge search space which made simulation time take 3 days to find WCTVs while the genetic algorithm take almost 5 minutes. Furthermore, the WCTVs for leakage current and delay failure which the genetic algorithm found are either optimum or near-optimum solutions.

The new methodologies for finding leakage current and delay failure WCTVs are validated experimentally using 8*8 multiplier chip and bridge chip respectively which were fabricated at MOSIS company using CMOS AMI 0.5 u technology and Mentor Graphics tools (Leonardo spectrum, fast scan, design architect and IC station). After that the chips were exposed to radiation using cobalt 6o device at the national center for radiation research and technology.

The test vectors which were generated using the genetic algorithm simulation were applied on the chips during radiation, and then leakage current and delay were measured. Nominal vectors which give average measurements for leakage current and delay were selected using exhaustive search to compare it with WCTVs. The comparison proved that there are significant between WCTVs and nominal vectors in measuring leakage current and delay after exposing the chips to radiation.

Chapter 1 : Introduction

In this thesis, the worst case test vectors (WCTV) that can be used to induce leakage current and delay failures in sequential circuits that are exposed to radiation are indentified. It`s importance lies in keeping the sequential circuits safe and working properly even when they are exposed to source of radiation by other methods instead of shielding circuits by any materials.

1.1. Introduction

When the electronic chips are exposed to source of radiation like space or x-rays, their function may not occur properly. This is due to the leakage current and delay failure that may happen when the chips are exposed to a certain amount of total dose.

There are many papers that discussed the effect of radiation on the combinational and sequential circuits in general and there are those which identified WCTVs that induced leakage current on the combinational circuits without talking about sequential ones. Therefore, in this thesis the effect of radiation on CMOS sequential circuits and identifies WCTVs that induced leakage current and delay failures on these circuits are discussed.

1.2. Motivation

The results of this thesis will be used to protect the sequential circuits from the leakage current and delay failures when exposed to the radiation. There are many ways to protect the electronics chips from radiation, one of them to shield the chip by material like lead with specific thickness but this method is expensive. Instead chips will be redesigned to use less sensitive cells to radiation consequently; they can be protected without using any shielding materials.

1.3. Problem Statement

The old papers focused on discussing the effect of radiation on electronic circuits only, by determining what occur to the chips after they exposed to radiation. This thesis will focus on identifying WCTVs that maximize leakage current and propagation delay on sequential circuits when they will be exposed to radiation.

1.4. Methodology

First in this thesis two fault models are developed. One of them calculates leakage current and the other one calculates propagation delay of sequential circuits. After that search for WCTVs that induced leakage current and delay failures is introduced using

genetic algorithm (GA). Finally our simulation results are validated using physical experiment. This physical experiment will used sequential and combinational chips that are designed using AMI 0.5 u CMOS technology by Mentor Graphics tools and fabricated at MOSIS. These chips then will be exposed to radiation rays using cobalt 60 device at national center for radiation research and technology.

1.5. Thesis Organization

The remainder of this thesis is organized as following. Chapter 2 will provide a description of electromagnetic spectrum, background on metal oxide semi conductor field effect transistor (MOSFET) and the radiation effect on MOSFET. After that chapter 3 will talk about the logic and leakage current fault model for sequential circuits and how to generate the WCTVs for them. The methodology for finding delay failure worst case test vectors will explain in chapter 4. Finally chapter 5 will conclude the thesis and will talk about our future work.