DESIGN FOR YIELD FOR SUB-22nm FinFET-BASED FPGA

By

Mohamed Mohie El-Din Mohamed Aly Hassan

A Thesis Submitted to the
Faculty of Engineering at Cairo University
in Partial Fulfillment of the
Requirements for the Degree of
MASTER OF SCIENCE
in
Electronics and Communications Engineering

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Title of Thesis:

Design For Yield For Sub-22nm FinFET-Based FPGA

Key Words:
Design for Yield; Process Variations; FPGA; Leakage Power

Summary:

In this thesis, a performance evaluation study for a FinFET-Based FPGA cluster under threshold voltage variation, representing the Die-to-Die variations, is launched with technology scaling starting from 20nm down to 7nm nodes showing the scaling trends of various performance metrics including the average power, delay, and power-delay product. Also some design insights and recommendations are proposed for the designers to achieve yield percentage of 99.87%. The leakage power is also studied for 14nm technology node under threshold voltage and temperature variations. Some solutions are implemented for leakage power control under threshold voltage variations including transistor stacking, minimum leakage vector, and gate sizing.

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Nomenclature

ADE	Analog Design Environment
ASIC	Application-Specific Integrated Circuits
BLE	Basic Logic Element
BSIM	Berkley Short-channel IGFET Model
CAD	Computer-Aided Design
CMG	Common Multi-Gate
CMOS	Complementary Metal-Oxide Semiconductor
DIBL	Drain-Induced Barrier Lowering
DLL	Delay-Locked Loop
D2D	Die-to-Die
FinFET	Fin Field Effect Transistor
FPGA	Field-Programmable Gate Array
GIDL	Gate-Induced Drain Leakage
IGFET	Independent-Gate FET
LER	Line-Edge Roughness
LSTP	Low Standby Power Devices
LUT	Look-Up Table
NWE	Narrow Width Effects
OPE	Optical Proximity Effects
PDF	Probability Density Function
PDP	Power-Delay Product
PLL	Phase-Locked Loop
RDF	Random Dopant Fluctuations
SCE	Short Channel Effects
SGFET	Shorted-Gate FET
SoPC	System-on-a-Programmable-Chip
SRAM	Static Random Access Memory
SSTA	Statistical Static Timing Analysis
WID	Within-Die

Abstract

As CMOS technology is scaled towards the deep sub-micron regime, digital circuits' designers are facing increased variability in form of either process variations or environmental variations. Those variations are classified to Die-to-Die variations and Within-Die variations. Our work presented in this thesis aims at evaluating the performance of a FinFET-Based FPGA cluster under threshold voltage variation that represents the Die-to-Die variations with technology scaling starting from 20nm down to 7nm nodes using Berkley Predictive Technology Models, showing the scaling trends of different performance metrics including the average power, delay, and power-delay product. Some design insights and recommendations are proposed for the designers to achieve yield percentage of 99.87%.

Since the leakage power is much more pronounced in advanced technology nodes, we also studied the leakage power and its variation for 14nm technology node under threshold voltage and temperature variations. The results emphasized the log-normal dependency of the leakage power on the threshold voltage and also the exponential dependency with temperature. Some solutions are proposed and implemented for leakage power control under threshold voltage variation including transistor stacking, minimum leakage vector (MLV), and gate sizing. These solutions have shown improvements for both the leakage power and leakage power variation, but also these solutions introduced a minor delay and area overheads which are reported and compared as well.

The FPGA cluster we built for our study is configured to a 2-bit adder benchmark used for both the performance evaluation study with technology scaling and the leakage power evaluation study as well. Cadence Virtuoso and ADE-GXL are used for both FPGA cluster building and simulations respectively.

Chapter 1 : Introduction

This chapter presents a short introduction about the significance of studying the effect of process variations while scaling down CMOS technologies coming to different FinFET technologies. Section 1.1 presents the motive behind this research work. Section 1.2 provides the thesis outline and organization.

1.1. Motivation

More than four decades of scaling CMOS technology has been the biggest driver for electronics industry. CMOS transistor scaling allowed building chips with billions of transistors in modern Integrated Circuits (ICs) and a broad range of electronic products with very high integration levels [1]. Nevertheless, the continued rigorous scaling of CMOS technology in sub-100nm regime has created massive design challenges, especially when transitioning to advanced technology nodes starting from 22nm technology. Assignable to process control limitations, manufacturing tolerances in process technology are not equally scaling as the transistor channel length [2-5]. Furthermore, process variations due to fundamental physical limits such as Line-End Roughness (LER) and Random Dopant Fluctuations (RDF) are significantly increasing with technology scaling [2, 6-11]. Consequently, statistical parameter variations are getting worse with consecutive technology generations, and variability is currently becoming one of the biggest challenges that face the semiconductor industry, resulting in huge yield losses [5]. That variability has been affecting analog design for some considerable time, and currently it is significantly impacting digital design at nanometer technology nodes. In addition, scaling the threshold voltage in nanometer regime posed a massive increase in the sub-threshold leakage current due to the exponential dependence, hence affecting the power efficiency which is becoming the key to sustaining continually enhanced performance for future VLSI circuits,

1.2. Organization of the Thesis

In order to have an overview about the process variations effects on the next generation FPGAs incorporating FinFETs devices in the manufacturing process, it is important to study the variations effects on the basic performance metrics such as the average power, delay, and power-delay product.
An introduction about the process variations in general, their sources and impacts on the digital circuits, is illustrated in Chapter 2. Chapter 3 gives an introduction about FPGAs, their structures, and the FPGA cluster we used for our study. It also contains the description of each unit comprising the FPGA cluster along with its simulation waveforms and measurements for basic performance metrics such as power, delay, and power-delay product (PDP).

In Chapter 4, we study the impact of threshold voltage variation with, representing D2D variations, with FinFET technology scaling from 20nm down to 7nm over the

FPGA cluster we built for our evaluation study. Also some design insights are presented in this chapter that help achieving a yield percentage of 99.87%.

Since the leakage power is becoming much more pronounced with the continued technology scaling, Chapter 5 presents the work done in order to study the leakage power variation with both the threshold voltage and temperature on the FPGA cluster. Also some solutions are proposed and implemented in order to control the leakage power for 14nm node.

And finally, the conclusion and the potential future work are drawn in "Discussion and Conclusions" section.

Appendix A illustrates the PTM models we used in our simulation in detail.