شبكة المعلومات الجامعية

بسم اللّه الرحمن الرحيم

شبكة المعلومات الجامعية

شبكة المعلومات الجامعية

التوثيق الالكتروني والميكروفيلم

شبكة المعلومات الجامعية

جامعة عين شمس

التوثيق الإلكتروني والميكروفيلم

قسم

نقسم باللّه العظيم أن المادة التي تم توثيقها وتسجيلها علي هذه الأقراص المدمجة قد أعدت دون أية تغيرات

يجب أن

تحفظ هذه الأقراص المدمجة بعيدا عن الغبار

شبكة المعلومات الجامعية

بعض الوثائق الأصلية تالفة

شبكة المعلومات الجامعية

بالرسالة صفحات
لم ترد بالأصل

Ain Shams University

Faculty of Engineering

Electronics and Communications Department

Phase-Locked Loop for High Speed Serial Data Links

A Thesis

Submitted in partial fulfillment for the requirements of Master of Science degree in Electrical Engineering

Submitted by:

Rania Hassan Mekky

B.Sc. of Electrical Engineering

(Electrical and Communications Department)

Ain Shams University, 2005.

Supervised by:

Prof. Dr. Magdy Mahmoud Ibrahim

Dr. Mohamed Amin Dessouky

Cairo 2009

Examiners Committee

Name: Rania Hassan Mekky
Thesis: Phase-Locked Loop for High Speed Serial Data Links
Degree: Master of Science in Electrical Engineering

Title, Name and Affiliation	Signature
Prof. Dr. Elsayed Mostafa Saad Helwan University, Faculty of Engineering, Electronics and Communications Department.	.....
Prof. Dr. Hani Fikry Ragai Ain Shams University, Faculty of Engineering, Electronics and Communications Department.	.....
Prof. Dr. Magdy Mahmoud Ibrahim Ain Shams University, Faculty of Engineering, Electronics and Communications Department.	.....
Dr. Mohamed Amin Dessouky Ain Shams University, Faculty of Engineering, Electronics and Communications Department.	.....

Date: 27/6/2009

Curriculum Vitae

Name: Rania Hassan Abdel Latif Abdel Rahim Mekky.
Date of Birth: 17/3/1984.
Place of Birth: Cairo, Egypt.
First University Degree: B.Sc. in Electrical Engineering.
Name of University: Ain Shams University.
Date of Degree: June 2005.

Statement

This dissertation is submitted to Ain Shams University for the degree of Master of Science in Electrical Engineering (Electronics and Communications Engineering).

The work included in this thesis was carried out by the author at the Electronics and Communications Engineering Department, Faculty of Engineering, Ain Shams University, Cairo, Egypt.

No part of this thesis was submitted for a degree or a qualification at any other university or institution.

Name: Rania Hassan Mekky.

Date: 21/3/2009.

Acknowledgment

All praise is due to Allah, Most Merciful, the Lord of the Worlds, Who taught man what he knew not. I would like to thank God Almighty for bestowing upon me the chance, strength and ability to complete this work.

I would like to express my thanks and gratitude to my advisers Prof.Dr Magdy Ibrahim and Dr. Mohamed Dessouky for their genuine guidance during my research.

I wish to thank Mentor Graphics Egypt for supporting me with all the needed resources to make my research during the period I worked for. Also I'd like to thank Newport Media for supporting especially the RF Team Dr. Hassan Elwan, Dr Ahmed Emira, Dr. Ahmed Nader and Mohamed Omar.

Finally, I would like to express my deepest appreciation to my family and my friends. In particular, I am always indebted to my parents for their constant support, love and patience. Without their continued support, I would have not accomplished this effort. I would like to thank my sister and two brothers for being so supportive and encouraging throughout years of my study.

Of course, I say first and foremost "Thanks to ALLAH".

To Mum and Dad.

Abstract

This thesis aims to introduce a design for a fully integrated low-jitter multi-standard phase-locked loop (PLL) used as multi-standard clock generator for Serializer-Deserializer (SerDes). The PLL is used for applications in frequency range of $0.8-6.3GHz$ with spread spectrum clocking feature to solve the electromagnetic interference (EMI) problem. For cost effect solution, fractional-N PLL is used to support the multi-standards such as PCI Express and XAUI with spread spectrum clocking for the SATA standard. Higher-order $\Sigma\Delta$ modulation reduces inband quantization noise by allowing the loop bandwidth to be increased without increasing the total phase noise. Third order $\Sigma\Delta$ MASH modulator is chosen. Forth order Type II charge pump PLL architecture is implemented. The loop type and order are determined based on system level design.

The SSCG supports the SATA I, II, III with 30 to 33 kHz triangular modulation profile and 5000 ppm frequency deviation with EMI reduction 20 dB.

Gain-boosting technique is used with charge pump (CP) to get low mismatch with wide compliance range.

For minimum area, ring oscillator is used as voltage-controlled oscillator (VCO). A multi-range VCO is proposed to handle the wide range of operation. Extended multi-modulus divider (MMD) is used to cover the wide devision ratios.

Switching activity in large digital systems introduces power supply or substrate noise which perturb the more sensitive blocks in a PLL, in particular, CP, VCOs and clock buffers. Two different supply domains are introduced, one for the sensitive blocks and the other one for the aggressor blocks. The block level design and implementation are demonstrated. Moreover, circuits' simulations, layouts and post layout simulations for each block as well as the complete system are introduced. The system can support operating frequency range from 0.8 to $6.3GHz$ with less than 6.5 ps rms jitter and power consumption of $7mW$ at $6.3GHz$. The PLL is implemented in 90nm CMOS generic technology. The CMOS generic technology is common used in industry for cost reasons. There are no inductors nor MIM capacitors used in the design, Only core, input-output devices and poly resistors are used. The capacitors are implemented using NMOS capacitors. The PLL occupies small area of 0.14x0.16 mm^2.

Contents