

# بسم الله الرحمن الرحيم





# شبكة المعلومات الجامعية

## التوثيق الالكتروني والميكروفيلم



# جامعة عين شمس

التوثيق الإلكتروني والميكرو فيلم

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**Ain Shams University**

**Faculty of Engineering**

**Electronics and Communications Department**

# **Phase-Locked Loop for High Speed Serial Data Links**

**A Thesis**

**Submitted in partial fulfillment for the requirements of Master of Science  
degree in Electrical Engineering**

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# Statement

This dissertation is submitted to Ain Shams University for the degree of Master of Science in Electrical Engineering (Electronics and Communications Engineering).

The work included in this thesis was carried out by the author at the Electronics and Communications Engineering Department, Faculty of Engineering, Ain Shams University, Cairo, Egypt.

No part of this thesis was submitted for a degree or a qualification at any other university or institution.

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# Abstract

This thesis aims to introduce a design for a fully integrated low-jitter multi-standard phase-locked loop (PLL) used as multi-standard clock generator for Serializer-Deserializer (SerDes). The PLL is used for applications in frequency range of  $0.8 - 6.3GHz$  with spread spectrum clocking feature to solve the electromagnetic interference (EMI) problem. For cost effect solution, fractional- $N$  PLL is used to support the multi-standards such as PCI Express and XAUI with spread spectrum clocking for the SATA standard. Higher-order  $\Sigma\Delta$  modulation reduces inband quantization noise by allowing the loop bandwidth to be increased without increasing the total phase noise. Third order  $\Sigma\Delta$  MASH modulator is chosen. Forth order Type II charge pump PLL architecture is implemented. The loop type and order are determined based on system level design.

The SSCG supports the SATA I, II, III with 30 to 33 kHz triangular modulation profile and 5000 ppm frequency deviation with EMI reduction 20 dB.

Gain-boosting technique is used with charge pump (CP) to get low mismatch with wide compliance range.

For minimum area, ring oscillator is used as voltage-controlled oscillator (VCO). A multi-range VCO is proposed to handle the wide range of operation. Extended multi-modulus divider (MMD) is used to cover the wide deviation ratios.

Switching activity in large digital systems introduces power supply or substrate noise which perturb the more sensitive blocks in a PLL, in particular, CP, VCOs and clock buffers. Two different supply domains are introduced, one for the sensitive blocks and the other one for the aggressor blocks. The block level design and implementation are demonstrated. Moreover, circuits' simulations, layouts and post layout simulations for each block as well as the complete system are introduced. The system can support operating frequency range from 0.8 to  $6.3GHz$  with less than 6.5 ps rms jitter and power consumption of  $7mW$  at  $6.3GHz$ . The PLL is implemented in 90nm CMOS generic technology. The CMOS generic technology is common used in industry for cost reasons. There are no inductors nor MIM capacitors used in the design, Only core, input-output devices and poly resistors are used. The capacitors are implemented using NMOS capacitors. The PLL occupies small area of  $0.14 \times 0.16 \text{ mm}^2$ .

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