AIN SHAMS UNIVERSITY
FACULTY OF ENGINEERING
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Electronics and Communications Engineering Department

Advanced Acquisition Techniques for Phase Locked Loops

A Thesis
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Submitted by

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STATEMENT

This thesis is submitted to Ain Shams University in partial fulfillment of the degree of Master of Science in Electrical Engineering.
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The work included in this thesis was carried out by the author in the integrated circuits laboratory of the Electronics and Communications Engineering Department, Faculty of Engineering, Ain Shams University, Cairo, Egypt.

No part of this thesis has been submitted for a degree or a qualification at any other university or institution.

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Abstract

Phase-locked loops (PLLs) have been used in many applications ranging from communications, radar to automobiles. In the recent past, digital phase-locked loops have been widely used in high-performance microprocessors and high-speed digital communication systems as clock generators. As the speed of these systems increasing, the PLLs with higher operating frequency and lower jitter are in demand. So in nearly all the PLL applications, it is required to generate low noise while achieve fast settling time. The settling time is largely determined by the loop bandwidth. In some applications, the loop bandwidth should be made as narrow as possible to minimize output phase jitter due to external noise, resulting in an elongated settling time. One of the solutions to this problem is the adaptive PLL using a wide bandwidth in the out-of-lock state and switching to a narrow bandwidth as the loop settles. With the adaptive PLL, one could speed up the settling process while ensuring sufficient reference feed-through attenuation for low output noise. In this thesis, extended loop bandwidth enhancement is achieved by the adaptive control on the loop filter resistances. Wide bandwidth is used when the PLL is in the out-of-lock state, while the narrow bandwidth is used when the PLL is in the lock state. This can be accomplished by applying different methods to change the loop filter resistance in the out-of-lock state. The change in the loop filter resistance depends on the difference between the input and the output frequencies; as this difference decreases, the resistance change to obtain smooth transition to lock. A frequency difference circuit is used to represents the difference between the input and output frequencies by a certain voltage to control the loop filter resistance. An industrial CMOS 4046 IC is used to implement the PLL, a lock time reduction up to 75% was achieved compared with the conventional PLL.

بسْــم الله الرَّحمَـن الرَّحيــم :

" وَعَلَّمَكَ مَا لَمْ تَكُنْ تَعْلَمُ وَكَانَ فَضْلُ اللَّهِ عليك عظيماً. "

صدق الله العظيم

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Dina M. El-Laithy

Abstract

Phase-locked loops (PLLs) have been used in many applications ranging from communications, radar to automobiles. In the recent past, digital phase-locked loops have been widely used in high-performance microprocessors and high-speed digital communication systems as clock generators. As the speed of these systems increasing, the PLLs with higher operating frequency and lower jitter are in demand. So in nearly all the PLL applications, it is required to generate low noise while achieve fast settling time. The settling time is largely determined by the loop bandwidth. In some applications, the loop bandwidth should be made as narrow as possible to minimize output phase jitter due to external noise, resulting in an elongated settling time. One of the solutions to this problem is the adaptive PLL using a wide bandwidth in the out-of-lock state and switching to a narrow bandwidth as the loop settles. With the adaptive PLL, one could speed up the settling process while ensuring sufficient reference feed-through attenuation for low output noise. In this thesis, extended loop bandwidth enhancement is achieved by the adaptive control on the loop filter resistances. Wide bandwidth is used when the PLL is in the out-of-lock state, while the narrow bandwidth is used when the PLL is in the lock state. This can be accomplished by applying different methods to change the loop filter resistance in the out-of-lock state. The change in the loop filter resistance depends on the difference between the input and the output frequencies; as this difference decreases, the resistance change to obtain smooth transition to lock. A frequency difference circuit is used to represents the difference between the input and output frequencies by a certain voltage to control the loop filter resistance. An industrial CMOS 4046 IC is used to implement the PLL, a lock time reduction up to 75% was achieved compared with the conventional PLL.

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