



**AIN SHAMS UNIVERSITY
FACULTY OF ENGINEERING
ELECTRONICS AND COMMUNICATIONS ENGINEERING DEPARTMENT**

Design of Voltage Controlled Oscillator (VCO) Based Analog-to-Digital Converter (ADC)

A Thesis

Submitted in Partial Fulfillment for Requirement of Master of Science
Degree in Electrical Engineering

Submitted by

Waleed Mohammed Abd El-Azem El-Halwagy

B.Sc. of Electrical Engineering
(Electronics and Communications Engineering)
Ain Shams University, 2009

Supervised by

Prof. Dr. Hassan Ahmed El-Ghitani

Dr. Mohammed Amin Dessouky

Cairo – Egypt

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No part of this thesis has been previously submitted for obtaining a degree or a qualification before.

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Abstract

In future technologies with low supply voltages and low headroom, the design of conventional voltage-based ADC is facing more difficulties due to the reduced voltage swing. On the other hand, the time resolution and the switching speed are improved. This makes the all digital VCO-Based ADC that utilizes the improved gate delay as its resolution more attractive in deep submicron technologies.

A programmable SWC-based VCO linearization feedback loop was proposed. Thorough analysis has led to clear guidelines for the choice of loop parameters. The main advantage of this linearization scheme is its programmability which makes this technique a suitable candidate in many applications. The loop was able to enhance the VCO linearity by a factor of 20. Also resolution enhancement techniques were invoked to improve the ADC resolution.

A nine-bit VCO-based ADC was implemented in the 130 nm CMOS process where the proposed programmable SWC-based VCO linearization technique was applied for SNDR enhancement. The proposed ADC employs a differential VCO coupling technique to enhance the VCO time resolution. The ADC can operate at sampling rates ranging from 130 MHz to 280 MHz with nominal sampling rate at 200 MHz. The 200MHz ADC was implemented in 130nm CMOS process showing an SNR/SNDR ranging from 91.4/88.3dB to 54.3/41.2dB for an input bandwidth of 500kHz – 100MHz while consuming a total of 8.3mW from a 1.2V supply. The loop improves the VCO linearity from 2% to 0.15%.

Keywords-voltage controlled oscillator (VCO); analog to digital converter (ADC); analog calibration; digital calibration; pseudo-differential; switched capacitor feedback; VCO linearization; negative skew; coupled VCO

Summary

The voltage-controlled oscillator (VCO) based analog-to-digital converter (ADC) is a digital approach for ADC implementation.. This thesis aims to introduce a design for a VCO-based ADC while applying a calibration technique to enhance the ADC linearity.

The thesis is divided into five chapters including lists of contents, tables and figures as well as list of references and one appendix.

Chapter 1

This chapter states the motivation for using time-based ADCs instead of the conventional voltage-based ones, as well as the need to apply a calibration technique for linearity improvement. The chapter ends with the thesis outline.

Chapter 2

In chapter 2, the Voltage Controlled Oscillator (VCO) Based Analog-to-Digital Converter (ADC) is introduced and analyzed. Also previous publications that covered this ADC architecture are presented.

Chapter 3

One of the important limitations in the design of the VCO-based ADC is the nonlinearity present in the VCO which results in degrading the SNDR of the ADC. In this chapter we shall introduce different techniques by which we can reduce the harmonic distortion and improve the linearity of the VCO-based ADC. Three linearity techniques will be invoked, namely, pseudo-differential configuration, foreground digital calibration and a switched capacitor feedback loop for VCO linearization.

Chapter 4

This chapter presents the behavioral modeling and simulation of the ADC while applying different calibration techniques for linearity improvement using CppSim and MATLAB.

Chapter 5

The design of the proposed VCO-based ADC implemented in 130 nm CMOS is presented. The proposed switched-capacitor feedback loop is used for linearizing the VCO characteristics and improving the SNDR of the ADC. In the end, a comparison with the state-of-the-art ADCs is introduced.

The thesis ends by conclusions, summary and future work.

Contents

ABSTRACT	iv
SUMMARY	v
CONTENTS	vi
LIST O FIGURES	ix
LIST OF TABLES	xviii
ACRONYMS	xx
CHAPTER 1. INTRODUCTION AND THESIS MOTIVATION	1
1.1 BACKGROUND AND MOTIVATION.....	1
1.2 THESIS OUTLINE	3
CHAPTER 2. VOLTAGE-CONTROLLED OSCILLATOR BASED ANALOG-TO-DIGITAL CONVERTER	4
2.1 INTRODUCTION	4
2.2 VOLTAGE-CONTROLLED OSCILLATOR.....	5
2.2.1 BASICS OF THE VOLTAGE-CONTROLLED OSCILLATOR.....	5
2.2.2 LINEARITY OF THE VOLTAGE-CONTROLLED OSCILLATOR.....	5
2.2.3 THE VOLTAGE-CONTROLLED OSCILLATOR AS A VOLTAGE – TO – PHASE INTEGRATOR.....	6
2.2.4 THE APPROPRIATE VCO TOPOLOGY TO BE USED IN THE ADC – THE RING VCO	7
2.3 THE DIFFERENT VOLTAGE-CONTROLLED OSCILLATOR BASED ADC ARCHITECTURES	7
2.3.1 THE SINGLE PHASE VCO-BASED ADC	8
2.3.2 THE INHERENT FIRST ORDER NOISE SHAPING OF THE VCO-BASED ADC	8
2.3.3 DRAWBACKS OF THE SINGLE PHASE VCO-BASED ADC	9
2.3.4 THE MULTI-PHASE VCO-BASED ADC	9
2.3.5 THE ONE BIT QUANTIZATION VCO-BASED ADC	10
2.4 SYSTEM MODELING AND SNDR LIMITATION FOR THE VCO-BASED ADC.....	12
2.4.1 LINEAR MODELING	12
2.4.2 SNDR LIMITATION DUE TO VCO NON-LINEARITY	13
2.5 RESOLUTION OF THE VCO-BASED ADC	13
2.5.1 RESOLUTION OF THE SINGLE PHASE VCO-BASED ADC	14
2.5.2 THE RESOLUTION OF THE MULTIPHASE QUANTIZER.....	16
2.5.3 THE RESOLUTION OF THE ONE BIT QUANTIZER	18
2.6 QUANTITATIVE ANALYSIS OF THE VCO-BASED ADC.....	19
2.6.1 NOISE SHAPING.....	19

2.6.2 NOISE SHAPING IN THE VCO-BASED ADC	20
2.6.3 THE PEAK SIGNAL-TO-QUANTIZATION NOISE RATIO OF THE VCO-BASED ADC.....	23
2.6.3.1 Compute the input power in the phase domain in the presence of S/H	24
2.6.3.2 Compute the input power in the phase domain in the absence of S/H	24
2.6.3.3 Compute the Variance (Power) of Quantization Noise	25
2.6.3.4 Computing the SQNR of the VCO-based ADC.....	27
2.7 THE DIFFERENCE BETWEEN MULTI-BIT AND ONE BIT QUANTIZATION.....	29
2.7.1 VCO QUANTIZERS CLASSIFICATION	29
2.7.2 DISTINGUISH BETWEEN MULTI-BIT AND ONE BIT VCO QUANTIZERS	33
2.7.3 PRACTICAL IMPLEMENTATION CONSIDERATIONS	33
2.7.4 VCO-BASED ADC DESIGN PERSPECTIVES – CASE STUDY	34
2.7.4.1 Multi-bit Quantizer Design	36
2.7.4.2 One Bit Quantizer Design	38
2.8 STATE – OF – THE – ART	38

CHAPTER 3. DIFFERENT TECHNIQUES TO REDUCE THE HARMONIC DISTORTION AND IMPROVE THE ADC RESOLUTION41

3.1 DISTORTION CANCELLATION VIA POLYPHASE MULTIPATH CIRCUITS	41
3.2 PSEUDO – DIFFERENTIAL ARCHITECTURE FOR LINEARITY IMPROVEMENT	44
3.2.1 PSEUDO – DIFFERENTIAL VCO-BASED ADC	44
3.2.2 RESULTS FROM PREVIOUSLY PUBLISHED PAPERS	44
3.3 FOREGROUND DIGITAL CALIBRATION OF VCO NON-LINEARITY	44
3.3.1 DIGITAL CALIBRATION TECHNIQUE DESCRIPTION	45
3.3.2 THE LUT SHOULD BE THE INVERSE FUNCTION OF THE VCO TUNING CURVE	45
3.3.3 MOVING AVERAGE IS APPLIED TO REDUCE QUANTIZATION NOISE	45
3.3.4 DESIGN PERSPECTIVES AND ILLUSTRATIVE EXAMPLE	47
3.3.5 RESULTS FROM PREVIOUSLY PUBLISHED PAPERS	49
3.4 SWITCHED CAPACITOR FREQUENCY CONTROL LOOP.....	49
3.4.1 THEORY OF OPERATION OF THE FREQUENCY CONTROL LOOP	50
3.4.2 QUANTITATIVE ANALYSIS OF THE FREQUENCY CONTROL LOOP	52
3.4.3 APPLICATIONS OF THE SWC FREQUENCY CONTROL LOOP	55
3.5 THE SWITCHED CAPACITOR VCO LINEARIZATION TECHNIQUE	56
3.5.1 SYSTEM DESCRIPTION	56
3.5.2 THEORY OF OPERATION	57
3.5.3 QUANTITATIVE ANALYSIS OF THE VCO LINEARIZATION LOOP.....	60
3.5.4 VCO LINEARIZATION LOOP DYNAMICS.....	64
3.5.5 VCO LINEARIZATION LOOP DESIGN PERSPECTIVES	65
3.5.5.1 The Inverse VCO Linearization Loop	65
3.5.5.2 The Direct VCO Linearization Loop	66
3.6 ADC RESOLUTION IMPROVEMENT TECHNIQUES.....	67
3.6.1 PASSIVE PHASE INTERPOLATION.....	67
3.6.2 NEGATIVE SKEWED DELAY SCHEME	70
3.6.3 COUPLED VOLTAGE CONTROLLED OSCILLATOR	73

CHAPTER 4. BEHAVIORAL MODELING AND SYSTEM LEVEL SIMULATIONS	77
4.1 INTRODUCTION	77
4.2 RING VOLTAGE CONTROLLED OSCILLATOR CIRCUIT LEVEL IMPLEMENTATION.....	77
4.2.1 TESTING THE DESIGN KIT FOR DIGITAL IMPLEMENTATION	78
4.2.2 DIFFERENT DELAY CELLS FOR THE RING VOLTAGE-CONTROLLED OSCILLATOR	81
4.2.2.1 Delay Cell Scheme 1: Current Starved Inverter Delay Cell	81
4.2.2.2 Delay Cell Scheme 2: DCVSL Inverter with Tail Current Source	83
4.2.2.3 Delay Cell Scheme 3: DCVSL Inverter with Parallel Current Source	84
4.2.2.4 Delay Cell Scheme 4: Pseudo-NMOS Inverter with PMOS Current Source	86
4.2.2.5 Choosing the Appropriate Delay Unit Scheme	88
4.3 BEHAVIORAL MODELING AND SIMULATION OF THE VCO-BASED ADC.....	88
4.3.1 SINGLE PHASE – MULTI-BIT VCO-BASED ADC	90
4.3.2 MULTIPHASE – MULTI-BIT VCO-BASED ADC	93
4.3.3 ONE BIT VCO-BASED ADC	99
4.3.4 A PROPOSED MODEL FOR THE MULTI-BIT QUANTIZERS	101
4.4 APPLYING LINEARITY IMPROVEMENT TECHNIQUES	103
4.4.1 PSEUDO – DIFFERENTIAL CONFIGURATION	105
4.4.2 FOREGROUND DIGITAL CALIBRATION TECHNIQUE	107
4.4.3 THE PROPOSED SWC FEEDBACK LOOP FOR VCO LINEARIZATION.....	112
4.5 BEHAVIORAL MODELING OF A LINEARIZED VCO-BASED ADC.....	121
4.5.1 APPLYING THE SWC FEEDBACK LINEARIZATION TECHNIQUE.....	122
4.5.2 APPLYING DIGITAL CALIBRATION TECHNIQUE	124
4.5.3 COMPARING ANALOG AND DIGITAL CALIBRATION TECHNIQUES	125
 CHAPTER 5. VOLTAGE CONTROLLED OSCILLATRO BASED ANALOG-TO-DIGITAL CONVERTER IMPLEMENTATION.....	 126
5.1 THE UNCALIBRATED VCO – BASED ADC	126
5.1.1 THE COUPLED VOLTAGE CONTROLLED OSCILLATOR	127
5.1.2 THE PHASE QUANTIZER	128
5.1.3 THE SINGLE PHASE VCO-BASED ADC	133
5.1.4 MULTI-PHASE SINGLE LEG VCO-BASED ADC	137
5.1.5 THE COMPLETE UNCALIBRATED VCO-BASED ADC	140
5.2 THE SWC FEEDBACK VCO LINEARIZATION LOOP	144
5.2.1 THE SWITCHED CAPACITOR NETWORK	144
5.2.2 THE OPERATIONAL TRANSCONDUCTANCE AMPLIFIER.....	145
5.2.3 DESIGN OF THE LINEARIZATION LOOP PARAMETERS.....	148
5.3 FINAL ADC SIMULATION RESULTS	150
5.4 COMPARISON	157
 CONCLUSION AND FUTURE WORK	 159
REFERENCES	160
APPENDIX A	165

List of Figures

Figure 1.1	Comparison between voltage-based and time-based ADCs and motivation to migrating to time-based ADCs.....	2
Figure 1.2	A plot of the ENOB versus technology scaling. The ENOB for 0.35 μ m CMOS process is set to zero [Kim 06].....	2
Figure 1.3	SNDR Degradation due to VCO-Nonlinearity.....	3
Figure 2.1	The Voltage Controlled Oscillator. [Razavi 00].....	5
Figure 2.2	The relation between phase and frequency for the VCO. [Razavi00]...	6
Figure 2.3	The VCO output phases. [Razavi 00].....	7
Figure 2.4	Illustrating the operation of the Single Phase VCO Based ADC. [Straayer1 08].....	8
Figure 2.5	The Inherent First Order Noise Shaping Property of the VCO Based ADC. [Straayer1 08].....	9
Figure 2.6	Illustrating the operation of the Multi Phase VCO Based ADC. [Park 09].....	9
Figure 2.7	The One Bit Quantization VCO Based ADC. [Park1 09].....	10
Figure 2.8	Block diagram model and corresponding linearized frequency domain model of the VCO based quantizer. [Park1 09].....	12
Figure 2.9	Behavioral Model illustrating the VCO Quantizer nonlinearity. [Straayer 08].....	13
Figure 2.10	Phase resolution for Single Phase Quantizer.....	15
Figure 2.11	Phase resolution for Multiphase Quantizer utilizing a three Stage Single ended VCO.....	16
Figure 2.12	The Phase Resolution for Multiphase Quantizer utilizing a three Stage differential VCO.....	17
Figure 2.13	The Phase Resolution for One Bit Quantizer utilizing a three Stage VCO.....	19

Figure 2.14	ADC Quantization Noise and Noise Shaping. [Maloberti 08].....	20
Figure 2.15	VCO-Based ADC with no S/H circuit before the VCO. [Kim1 10]....	21
Figure 2.16	The probability distribution function of the quantization noise.....	26
Figure 2.17	Plotting the Peak SQNR as a function of the ADC resolution (N_{bits}) and the Oversampling Ratio (OSR), assuming the presence of the Sample and Hold (S/H) circuit.....	31
Figure 2.18	A Plot of the Oversampling Ratio (OSR) versus the Sampling frequency while varying the bandwidth (BW).....	32
Figure 2.19	A Plot of the Sinc Filter in case the Sample and Hold (S/H) is absent.....	32
Figure 2.20	Different VCO Quantizers.....	33
Figure 2.21	A Plot showing the variation of the VCO number of stages - tuning range product as a function of the ADC resolution and sampling frequency.....	35
Figure 2.22	The VCO tuning range versus number of VCO stages that satisfies the maximum VCO product term requirement of 20 GHz.....	37
Figure 2.23	A Plot of the counter bit width versus the VCO number of stages.....	37
Figure 3.1	Polyphase multipath circuit for distortion cancellation [Yoon 09]...	42
Figure 3.2	Pseudo differential ADC architecture.....	44
Figure 3.3	Digital calibration for VCO nonlinearity [Kim1 10].....	46
Figure 3.4	Explanation of the MAF Operation.....	46
Figure 3.5	Illustrative Example for digital calibration.....	48
Figure 3.6	The block diagram of the switched capacitor frequency control loop.....	50
Figure 3.7	The timing waveforms of the frequency control loop including the integrator output and the VCO output clocks.....	51
Figure 3.8	Input Circuit arrangements for the Frequency Control Loop.....	56
Figure 3.9	Block diagram for the VCO linearization loop.....	57

Figure 3.10	The circuit schematic of the direct-VCO linearization loop.....	58
Figure 3.11	The timing waveforms for the direct VCO loop.....	58
Figure 3.12	The circuit schematic of the inverse-VCO linearization loop.....	59
Figure 3.13	The timing waveforms for the inverse VCO loop.....	59
Figure 3.14	Passive interpolation.....	68
Figure 3.15	The Seven Stage differential PDCVSL-PCS VCO test bench used to simulate the passive phase interpolation scheme.....	69
Figure 3.16	The 14 phases of the seven Stage differential PDCVSL-PCS VCO plotted before applying interpolation. (P1 and P2c are shown in black, while other phases are plotted in grey).....	69
Figure 3.17	Simulation results for the passive phase interpolation with $R = 1\text{k}\Omega$ interpolating resistor and 3 GHz oscillation frequency. (P1 and P2c are shown in black, while Pint is given in red).....	69
Figure 3.18	Simulation results for the passive phase interpolation with $R = 50\text{ k}\Omega$ interpolating resistor.....	70
Figure 3.19	The concept of the negative – skewed delay scheme.....	70
Figure 3.20	Simulation results of the negative-skewed inverter with the PMOS input leading that of the NMOS by 20 ps.....	72
Figure 3.21	A plot of t_{PLH} , t_{PHL} and the average power of the skewed inverter as a function of the negative skew.....	72
Figure 3.22	The skewed PDCVSL-PCS delay cell.....	74
Figure 3.23	The Skewed PDCVSL-PCS VCO Simulation results.....	74
Figure 3.24	The ten phases of the skewed five stage differential VCO.....	75
Figure 3.25	Schematic of the 5-stage 3-rung coupled ring oscillator.....	75
Figure 3.26	The coupled PDCVSL-PCS VCO delay unit.....	76
Figure 3.27	The 5x3 PDCVSL-PCS coupled VCO Simulation Results.....	76
Figure 4.1	The I-V characteristics of the NMOS and PMOS when operated in the digital mode.....	78

Figure 4.2	Inverter Simulations.....	79
Figure 4.3	Simulation results of the five stage ring oscillator.....	80
Figure 4.4	Current starved inverter delay cell for the VCO.....	82
Figure 4.5	NMOS controlled Current Starved Inverter after adding the control PMOS to the stack.....	82
Figure 4.6	The Simulation results of the five stage VCO utilizing a PMOS controlled Current Starved – Inverse VCO delay cell.....	82
Figure 4.7	DCVSL Inverter Schematic.....	83
Figure 4.8	Simulation results of the five stage differential ring oscillator.....	84
Figure 4.9	The ten output phases of the five stages differential ring oscillator....	85
Figure 4.10	The PMOS-cascode DCVSL with NMOS tail current source delay unit.....	85
Figure 4.11	The DIPCS Delay Unit Schematic.....	85
Figure 4.12	Simulation results of the five-stage VCO utilizing the PDCVSL – PCS delay unit.....	87
Figure 4.13	Simulation results of the five-stage VCO utilizing the NDCVSL – NCS delay unit.....	87
Figure 4.14	Simulation results of the five-stage VCO utilizing the PDCVSL – PNCS delay unit.....	87
Figure 4.15	The Pseudo-NMOS delay cell.....	88
Figure 4.16	The Algorithm used for behavioral modeling and simulation.....	89
Figure 4.17	Tuning Curve of the 7 Stage VCO utilizing DIPCS delay unit.....	90
Figure 4.18	Tuning Curve of the 31 Stage VCO utilizing DIPCS delay unit.....	90
Figure 4.19	The CppSim block diagram for the Single Phase – Multi-bit VCO based ADC.....	91
Figure 4.20	Timing waveforms of the single phase VCO-based ADC utilizing the PDCVSL – PCS delay unit.....	91

Figure 4.21	FFT plots of the single phase VCO-based ADC using DIPCS delay cells.....	92
Figure 4.22	The CppSim block diagram for the Multi-phase – Multi-bit VCO based ADC.....	94
Figure 4.23	Timing waveforms of the Multi-phase – Multi-bit VCO-based ADC utilizing the PDCVSL – PCS delay unit.....	95
Figure 4.24	FFT plots of the Multi-phase – Multi-bit VCO-based ADC using DIPCS delay cells for linear (black) and non-linear (grey) VCOs.....	96
Figure 4.25	A Plot of the ADC Resolution and SNDR versus Sampling Frequency.....	97
Figure 4.26	A Plot of the VCO tuning range and ADC Resolution versus the number of VCO stages.....	97
Figure 4.27	The CppSim block diagram for the One bit VCO based ADC.....	98
Figure 4.28	Timing waveforms of the One bit VCO-based ADC utilizing the PDCVSL – PCS delay unit.....	99
Figure 4.29	FFT plots of the One bit VCO-based ADC using DIPCS delay cells.....	100
Figure 4.30	Extracting a Model for the One-Bit VCO based ADC.....	101
Figure 4.31	Simulation results for the coded one-bit quantizer.....	102
Figure 4.32	FFT response of the coded one-bit quantizer output using the PDCVSL-PCS delay cell.....	102
Figure 4.33	The VCO tuning curve, average power and non-linearity.....	104
Figure 4.34	FFT plots of the MPMB VCO-based ADC using DIPCS delay.....	105
Figure 4.35	The CppSim Model for the Pseudo-differential VCO-based ADC configuration.....	106
Figure 4.36	Timing waveforms of the Pseudo-differential PDCVSL-PCS VCO-based ADC.....	106
Figure 4.37	FFT plots of the MPMB VCO-based ADC using DIPCS delay.....	107
Figure 4.38	The CppSim Model for foreground digital calibration and LUT extraction.....	108