AIN SHAMS UNIVERSITY
FACULTY OF ENGINEERING
ELECTRONICS AND COMMUNICATIONS ENGINEERING DEPARTMENT

Design of Voltage Controlled Oscillator (VCO) Based Analog-to-Digital Converter (ADC)

A Thesis

Submitted in Partial Fulfillment for Requirement of Master of Science Degree in Electrical Engineering

Submitted by

Waleed Mohammed Abd El-Azem El-Halwagy

B.Sc. of Electrical Engineering
(Electronics and Communications Engineering)
Ain Shams University, 2009

Supervised by

Prof. Dr. Hassan Ahmed El-Ghitani

Dr. Mohammed Amin Dessouky

Cairo – Egypt

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Curriculum Vitae

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Statement

This thesis is submitted to Ain Shams University in partial fulfillment of the Master of Science degree in Electrical Engineering

No part of this thesis has been previously submitted for obtaining a degree or a qualification before.

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Abstract

In future technologies with low supply voltages and low headroom, the design of conventional voltage-based ADC is facing more difficulties due to the reduced voltage swing. On the other hand, the time resolution and the switching speed are improved. This makes the all digital VCO-Based ADC that utilizes the improved gate delay as its resolution more attractive in deep submicron technologies.

A programmable SWC-based VCO linearization feedback loop was proposed. Thorough analysis has led to clear guidelines for the choice of loop parameters. The main advantage of this linearization scheme is its programmability which makes this technique a suitable candidate in many applications. The loop was able to enhance the VCO linearity by a factor of 20. Also resolution enhancement techniques were invoked to improve the ADC resolution.

A nine-bit VCO-based ADC was implemented in the 130 nm CMOS process where the proposed programmable SWC-based VCO linearization technique was applied for SNDR enhancement. The proposed ADC employs a differential VCO coupling technique to enhance the VCO time resolution. The ADC can operate at sampling rates ranging from 130 MHz to 280 MHz with nominal sampling rate at 200 MHz. The 200MHz ADC was implemented in 130nm CMOS process showing an SNR/SNDR ranging from 91.4/88.3dB to 54.3/41.2dB for an input bandwidth of 500kHz – 100MHz while consuming a total of 8.3mW from a 1.2V supply. The loop improves the VCO linearity from 2% to 0.15%.

Keywords-voltage controlled oscillator (VCO); analog to digital converter (ADC); analog calibration; digital calibration; pseudo-differential; switched capacitor feedback; VCO linearization; negative skew; coupled VCO

Summary

The voltage-controlled oscillator (VCO) based analog-to-digital converter (ADC) is a digital approach for ADC implementation.. This thesis aims to introduce a design for a VCO-based ADC while applying a calibration technique to enhance the ADC linearity.

The thesis is divided into five chapters including lists of contents, tables and figures as well as list of references and one appendix.

<u>Chapter 1</u>

This chapter states the motivation for using time-based ADCs instead of the conventional voltage-based ones, as well as the need to apply a calibration technique for linearity improvement. The chapter ends with the thesis outline.

<u>Chapter 2</u>

In chapter 2, the Voltage Controlled Oscillator (VCO) Based Analog-to-Digital Converter (ADC) is introduced and analyzed. Also previous publications that covered this ADC architecture are presented.

<u>Chapter 3</u>

One of the important limitations in the design of the VCO-based ADC is the nonlinearity present in the VCO which results in degrading the SNDR of the ADC. In this chapter we shall introduce different techniques by which we can reduce the harmonic distortion and improve the linearity of the VCO-based ADC. Three linearity techniques will be invoked, namely, pseudo-differential configuration, foreground digital calibration and a switched capacitor feedback loop for VCO linearization.

<u>Chapter 4</u>

This chapter presents the behavioral modeling and simulation of the ADC while applying different calibration techniques for linearity improvement using CppSim and MATLAB.

<u>Chapter 5</u>

The design of the proposed VCO-based ADC implemented in 130 nm CMOS is presented. The proposed switched-capacitor feedback loop is used for linearizing the VCO characteristics and improving the SNDR of the ADC. In the end, a comparison with the state-of-the-art ADCs is introduced.

The thesis ends by conclusions, summary and future work.

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