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FPGA Implementation of Digital Image Enhancement Techniques

Thesis submitted in partial fulfillment of the requirement for the degree of Master of Science

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Statement

This thesis is submitted in the partial fulfillment of master degree in Electrical Engineering to Ain Shams University.

The author carried out the work included in this thesis, and no part of this thesis has been submitted for a degree or qualification at any other university.

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ABSTRACT

The thesis proposes fast, flexible and reasonable development cost system of image enhancement technique using FPGA implementation. Several image enhancement techniques have been surveyed. Afterwards, select some of these techniques to implement using FPGA technology, and then results are analyzed and compared with software simulation results obtained before.

Research plan:

1- Literature survey in FPGA and digital image enhancement techniques.

2- Software implementation of the selected image enhancement techniques.

3- Hardware implementation of the selected techniques using FPGA.

4- Comparative study between the implemented software & hardware image enhancement techniques.

5- Conclusions and Future work.

Table of Contents

List of Abbreviation

DSP	Digital Signal Processor
ASIC	Application Specific Integrated Circuits
FPGA	Field Programmable Gate Arrays
LE	Logic Elements
PROM	Programmable Read-Only Memory
LUT	Look-Up Table
SRAM	Static Random-Access Memory
LAB	Logic Array Blocks
HDL	Hardware Description Language
VHDL	VHSIC Hardware Description Language
AHDL	Altera Hardware Description Layer
RTL	Register Transfer Level
EEPROM	Electrically Erasable Programmable Read-Only Memory
S/W	Software
H/W	Hardware

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Chapter 1
Introduction

Image Enhancement is a wide area with its applications in different domains. Image Enhancement is a very high computational process; in which processing involves applying a specific function repetitively. One solution to apply this computational process is to use a general-purpose microprocessor or Digital Signal processors. But these implementations are sequential, with less on chip memory for buffering, so we require external memory for buffering. Fetching data from this external memory require certain clock cycles which affect system performance. Also, these systems require a logic element for their operations. We can reduce this logic element and speed up our operations using Application Specific Integrated Circuits (ASICs). But main problems with ASICs, are that they require large time to market, and the initial investments are high. Before developing an ASIC, we require to prototype our design. Field programmable Gate Arrays (FPGAs) prove to be a better solution for rapid prototyping. FPGAs are reprogrammable, have large number of logic cells suitable for implementing image enhancement applications.

This thesis addresses the implementation of image enhancement algorithms like histogram equalization, contrast stretching, negative image transformation, power law transformation, and median filter on FPGA that have become a competitive alternative for high-performance digital signal processing applications. All implemented enhancement algorithms deal with spatial domain techniques, where they enhance low image contrast & remove impulse noise (Salt & paper noise) effectively. All the implementation work has been done in MATLAB 9.0, Quartus II, Xilinx software and DE0 board (Altera) & Spartan3 (Xilinx) [Hardware].

This thesis is organized in five chapters including this one. Chapter 2 introduces FPGA architecture, requirements of the FPGA hardware platform, FPGA design flow and Programming Languages, then background of image enhancement techniques in both spatial domain and frequency domain, and survey on implemented algorithms in spatial domain finally; some related work for Spatial Domain image enhancement techniques based on FPGA is introduced. Chapter 3 also presents software and hardware implementation of a five image enhancement algorithms like processing steps, Block diagram, Schematic diagram, loading image using RS232 and MATLAB code. Chapter 4 is going to show the performance analysis of the proposed hardware design in terms of computation speed, power consumption, and number of logic element in both (Altera - Xilinx) boards. In Chapter 5, the conclusion and future work discuss the thesis and all the work done. Further improvements and other ideas are suggested.

Chapter 2
Background and Literature survey

2.1 Introduction

This Chapter will introduce a background material relevant to the subject of this thesis. It begins by briery outlining FPGA architecture, FPGA design flow and Programming Languages. We then provide relevant technical details of image enhancement techniques in both spatial domain and frequency domain and survey on implemented algorithms in spatial domain used in this research. Finally we will outline related previous work for Spatial Domain image enhancement techniques based on FPGA.

2.2 FPGA Architecture

The Field Programmable Gate Array (FPGA) is a semiconductor device that can be programmed after manufacturing. We can use an FPGA to implement any logical function that an application-specific integrated circuit (ASIC) could perform, but the ability to update the functionality after shipping offers advantages for many applications [1].

The general architecture of FPGA is given in Figure 2.1. It consists of an array of programmable logic blocks of different types, including general logic, memory and multiplier blocks, surrounded by a programmable routing fabric that allows blocks to be programmable interconnected.

The array is surrounded by programmable input/output blocks, labeled I/O in the figure, that connect the chip to the outside world. The “programmable” term in FPGA indicates an ability to program a function into the chip after silicon fabrication is complete.

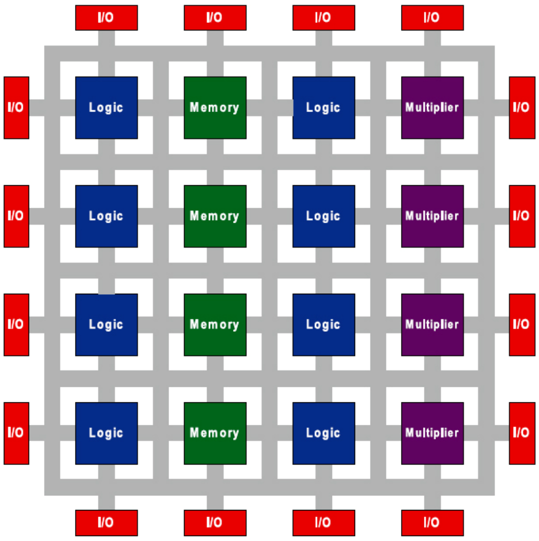

Figure 2.1 Basic hardware architecture of FPGA devices [2]

This change in function is made possible by the programming technology, which is a method that can cause a change in the behavior of the pre-fabricated chip after fabrication.

Unlike previous generation of FPGAs using I/Os with programmable logic and interconnects, today's FPGAs consist of various mixes of configurable embedded SRAM, high-speed transceivers, high-speed I/Os, logic blocks, and logic elements [1].

An FPGA contains a large number of logic elements (LE) that can be wired according to a logic function specified by a user defined code. Each element is interconnected by a matrix of wires and programmable switches. This is done by a user program that defines the function of the circuit, using a hardware description language such as Verilog or VHDL.

We can configure LE to perform complex combinational functions, or simple logic gates like AND, OR and XOR. In most FPGAs, the logic blocks also include memory elements, which may be simple flip flops or more complete blocks of memory.