**AIN SHAMS UNIVERSITY**
**FACULTY OF ENGINEERING**
**CAIRO – EGYPT**
**Electronics and Communications Engineering Department**

# Design & Implementation of Ethernet Medium Access Controller (MAC)

A Thesis
Submitted in partial fulfillment for the requirements of the degree
of **Master of Science in Electrical Engineering**

Submitted by

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Thesis: **Design & Implementation of Ethernet Medium Access Controller (MAC)**

Degree: **Master of Science in Electrical Engineering (Electronics and Communications Engineering)**

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Date: **27 / 5 / 2013**

# STATEMENT

This Thesis is submitted to Ain Shams University in partial fulfillment of the degree of Master of Science in Electrical Engineering.

The work included in this thesis was carried out by the author in the department of electronics and communications engineering, Ain Shams University.

No part of this Thesis has been submitted for a degree or a qualification at any other university or institute.

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### *To My Family*

*You make me reach this successful step in my life*

*I present to you this thesis*

*May I by this express my deep gratitude and love*

*Thanks*

Ain Shams University - Faculty of Engineering
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Thesis title:     "Design & Implementation of Ethernet Medium
                  Access Controller (MAC)"


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Summary

This thesis consists of the design, simulation and implementation of the simplified Ethernet MAC layer that can be used for the local access networks. The design was aimed to match the IEEE 802.3ah standard specification of the Ethernet In The First Mile "EFM" that is used with the EPON fiber local access networks.

The thesis is composed of five chapters together with the table of contents, the list of figures, tables and acronyms, the appendices, the references and the list of publications.

The thesis contents are presented hereafter:

   Chapter 1 presents the introduction to the thesis and displays the main reason that motivated the work of this thesis which is the increasing demand for providing higher bit rate communication within the subscriber access network (local loop) that leads to the future requirement of deploying the fiber networks. A comparison between the passive and active optical networks was established to show the advantages of the passive type (PON). After that, this chapter discusses the Gigabit PON (GPON) and Ethernet PON (EPON) flavors of the passive optical networks and gives reasons why EPON is preferred for future use. Hence, a spot light was put on the EPON networks showing its original dependency on the IEEE standard called Ethernet In the First Mile "EFM" and its architecture mapping to the OSI model. Also it discusses the transmission principle as well as the structure of the Optical Network Unit "ONU" and the Optical Line Terminal "OLT" units.  The second half of this chapter presents a "literature review" to show the previous work done in the field of EPON networks besides explaining the contribution and objectives of this thesis. Finally, it shows the schedule that has been followed during my work and a brief summery about the thesis achievements.

   Chapter 2 presents a detailed functional description of the MAC according to the IEEE 802.3ah standard. It begins with explaining the main difference between the old Ethernet frame format and the new format for EFM showing how the preamble field has been modified to handle the P2MP emulation required for EPON networks. Then it gives detailed definitions for the other frame fields including the MAC "Source" and "Destination" addresses, frame length/type, "Data & Padding" field and finally the "FCS" field. After that this chapter demonstrates the operation of the "Simplified MAC" as stated by the IEEE 802.3ah standard in both "Send" and "Receive" ways. Finally this chapter shows a sketch diagram of the MAC functions.

   Chapter 3 demonstrates the design phases that have been done during designing the EPON MAC IP. It starts with the "Interfaces Design" to specify the buses between the MAC

and other layers showing how the MAC interacts with the host side, streaming side and the PHY side. Then this chapter shows the "Structural Design" of the MAC by breaking it out into its building components giving functional explanation of each one. After that this chapter talks in details about the "Components Design" for both Tx & Rx Finite State Machines showing the hierarchal level mapped to the frame format then it gives complete description of every sub-state and transitions with the associated actions and conditions. In addition this chapter explains the design of other components like the P2MP Emulation Layer, Medium Management Unit, CRC generators and checkers, the register file and the loopback facilities.

Chapter 4 presents the effort done to build the simulation and verification environment. It shows the structure design of the Testbench containing my EPON MAC IP as the Unit Under Test "UUT" together with a functional model for the gigabit PHY layer besides using ready Bus Functional Models "BFM" form Altera Company to act as the LLC layer. Also, this chapter discusses the Testcases that have been performed on the EPON MAC IP in order to check its functionality in both normal and extreme operating conditions. In additions, it illustrates the simulation results with explanation for each Testcase.

Chapter 5 shows the work done in order to validate the MAC IP that have been designed. The validation was done by involving the MAC IP in a bigger network system such that we can perform live network operation. It was decided to do complete HW design for a PCI-based Network Interface Card that utilizes my designed MAC together with some other IPs from Altera to implement the LLC sublayer thus we could achieve complete implementation of the DLL layer. This chapter starts by giving an overview on the whole system explaining the interaction between the NIC card and the host processor and the mechanism used to transfer the Ethernet packets in both Tx and Rx directions. Then it presents a structural design of the NIC card showing the features of the IP's and how each one is configured to match the required specifications of my application. Then the integration of the system is done and the implementation results are shown. Finally, the SW development of the Linux device driver is presented with detailed description of the driver operation that is depicted by the flowcharts.

Finally, the thesis ends by extracting conclusions and stating future work that might be done based on this work. Then it involves a list of the references and publications that have been used during my research besides a CD disk contains the original thesis document with all design files & source codes.

# ACKNOWLEDGMENTS

## All gratitude to ALLAH

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