التخصص : الهندسة الكهربية
القسم : هندسة الإلكترونيات والإتصالات الكهربية
الدرجة : الماجستير

محمد أحمد محمد مصطفى سلام

الكود	:		
تاريخ الميلاد	:	٢٨ سبتمبر ١٩٨٤	
البكالوريوس	:	يوليو ٢٠٠٧	جامعة : عين شمس
الماجستير	:	يونيو ٢٠١٥	جامعة : عين شمس
تاريخ منح الدرجة	:		

هيئة الإشراف

ا د / محمد أمين دسوقى
ا د / محمد واثق الخراشى

لجنة الفحص و الحكم

ا د/ خالد على شحاتة
ا د/ أشرف محمد سالم
ا د / محمد أمين دسوقى
ا د / محمد واثق الخراشى

الشبكات الموثوقة وادارة الهوية

كلما زادت دقة تكنولوجيا التصنيع، زادت مشاكل التأخر فى الأسلاك الموصلة داخل النظم علي الرقاقة System-On-Chip (SoC) وخاصة الكبيرة منها.

الشبكات على الرقائق Networks-on-Chips (NoC) تعتبر حل للاتصالات داخل النظم علي الرقاقة الكبيرة. وهي تستخدم فكرة التواصل المتزامن محليا والتواصل الغير متزامن بين مختلف النوي عبر الرقاقة.

الاتصال ثم الائتمان Connection-then-Credit (CTC) هو بروتوكول للتحكم في تدفق المعلومات بين نقطتي البداية و النهاية فى الشبكات على الرقاقة. هذا البروتوكول يعتبر امتداد لبروتوكولات التحكم القائمه على الائتمان Credit-Based Flow Control (CB). بروتوكول الاتصال ثم الائتمان (CTC) تم تقديمه لمعالجة مشكلة توقف التدفق نتيجه الاعتماد المتبادل في الشبكات على الرقائق. بينما يقدم افضلية في الكفاءة المساحية بالمقارنة ببروتوكولات التحكم القائمة على الائتمان و التي تتطلب مساحات اكبر لتخزين المعلومات.

الهدف من هذه الرسالة هو تقديم تنفيذ جديد لكلا النوعين من البروتوكولات. كما تهدف هذه الرسالة لابراز كيفية تصميم و تخليق هذه البروتوكولات على تكنولوجيا TSMC ٤٠ نانوميتروبيان الافضلية المساحية لبروتوكول الاتصال ثم الائتمان CTC علي بروتوكول الائتمان العادي CB.

وقد تم تحليل نتائج التنفيذ لكلا النوعين من البروتوكولات و مقارنتهم باستخدام المعايير المعروفة لقياس سرعة تدفق المعلومات و ذلك عبر تنفيذ شبكة متكاملة على الرقاقة و التي تحتوي على واجهه شبكية و موزع شبكي و موصلات شبكية موزعة على شبكة طوبولوجيا.

An Area Efficient NoC Physical Layer

As the fabrication technology scales down, wire delays began to dominate gate delays. Consequently, global wires interconnecting the processing cores in a large System-On-Chip (SoC) became bottle-necks in its performance.

Networks-On-Chips (NoC) is a unified scalable intra-chip communication solution for large SoCs, employing Globally Asynchronous Locally Synchronous (GALS) concept in which locally synchronous cores are communicating asynchronously.

The Connection-Then-Credit (CTC) end-to-end flow control protocol is an extension to the normal Credit-Based (CB) flow control protocol that is widely used in NoC. CTC was introduced to address the NoC message-dependent deadlock problem, while offering an area-efficient network interface with respect to the normal CB flow control, which needs a lot of buffering resources.

The aim of this thesis is to present a cycle-accurate RTL design details of NoC Interfaces based on the CTC and the CB protocols. We also present their post-synthesis implementation results in TSMC 40nm CMOS technology, to highlight the area savings introduced by the CTC over the CB.

AIN SHAMS UNIVERSITY

FACULTY OF ENGINEERING

Electronics and Communications Engineering Department

An Area Efficient NoC Physical Layer

A Thesis submitted in partial fulfilment of the requirements of the degree of

Master of Science in Electrical Engineering

(Electronics and Communications Engineering)

Submitted by

Mohamed Ahmed Mohamed Mostafa Sallam

Bachelor of Science in Electrical Engineering

(Electronics and Communications Engineering)

Faculty of Engineering, Ain Shams University, 2007

Supervised by

Prof. Mohamed Amin Dessouky

Prof. Mohamed Watheq El-Kharashi

Cairo - (2015)

AIN SHAMS UNIVERSITY

FACULTY OF ENGINEERING

Electronics and Communications Engineering Department

An Area Efficient NoC Physical Layer

Submitted by

Mohamed Ahmed Mohamed Mostafa Sallam

Bachelor of Science in Electrical Engineering

(Electronics and Communications Engineering)

Faculty of Engineering, Ain Shams University, 2007

Examiners' Committee

Name and Affiliation **Signature**

Prof. Khaled Ali Shehata
Electronics and Communications ,
Arab Academy for Science, Technology,
and Maritime Transport

Prof. Ashraf Mohamed Salem
Computer and Systems ,
Ain Shams University

Prof. Mohamed Amin Dessouky
Electronics and Communications ,
Ain Shams University

Prof. Mohamed Watheq El-Kharashi
Computer and Systems ,
Ain Shams University

Date: /06/2015

Statement

This thesis is submitted as a partial fulfilment of Master of Science in Electrical Engineering Engineering, Faculty of Engineering, Ain shams University.

The author carried out the work included in this thesis, and no part of it has been submitted for a degree or a qualification at any other scientific entity.

Mohamed Ahmed Mohamed Mostafa Sallam

Signature

…………...……….

Date: /06/2015

Researcher Data

Name : Mohamed Ahmed Mohamed Mostafa Sallam

Date of birth : 28/09/1984

Place of birth : Cairo

Last academic degree : Bachelor of Science in Electrical Engineering

Field of specialization : Electronics and Communications

University issued the degree: Ain Shams University

Date of issued degree : July 2007

Current job : Sr. VLSI Design Engineer at Atmel Corporation

Abstract

As the fabrication technology scales down, wire delays began to dominate gate delays. Consequently, global wires interconnecting the processing cores in a large System-On-Chip (SoC) became bottle-necks in its performance. It became even harder to achieve global synchronization across the chip. Additionally, routing congestion problems increased with the tremendous increase in the number of communicating cores in a single SoC.

Networks-On-Chips (NoC) is a unified scalable intra-chip communication solution for large SoCs, employing Globally Asynchronous Locally Synchronous (GALS) concept in which locally synchronous cores are communicating asynchronously.

Although NoC design paradigm has a lot of performance advantages in terms of speed, power, scalability, reusability and time-to-market, however the global communication bandwidth offered by any NoC is still finite, where heavy traffic loads that causes contention of the NoC resources may result in an unpredictable latency. End-to-end flow control protocols are used to regulate the access to the NoC fabric, in a way that prevents the resources congestion while satisfying the Quality-of-Service (QoS) guarantees required by any system.

The Connection-Then-Credit (CTC) end-to-end flow control protocol is an extension to the normal Credit-Based (CB) flow control protocol that is widely used in NoC. CTC was introduced to address the NoC message-dependent deadlock problem, while offering an area-efficient network interface with respect to the normal CB flow control, which needs a lot of buffering resources.

The aim of this thesis is to present a cycle-accurate RTL design details of NoC Interfaces based on the CTC and the CB protocols. We also present their post-synthesis implementation results in TSMC 40nm CMOS technology, to highlight the area savings introduced by the CTC over the CB.

Keywords: Credit-based flow control, end-to-end protocol, message-dependent deadlock, network-interface, networks-on-chips.

Thesis Summary

In this thesis, the RTL design and implementation details of a complete NoC system will be presented. The NoC is a mesh-topology based, its routers employ worm-hole switching, XY-routing algorithm and round-robin arbitration, and the interfaces implement the CTC end-to-end flow control protocol. The NoC implementation is done using 40nm CMOS technology.

The thesis is divided into six chapters and lists of contents, tables, and figures as well as the bibliography and three appendices.

Chapter One: In this chapter, we give a brief introduction to the thesis and the research area of interest.

Chapter Two: In this chapter, the Networks-On-Chip concept is introduced, and its advantages, disadvantages, and implementation challenges are highlighted. It also presents the literature survey of different NoC interfaces implementation and different end-to-end flow control protocols.

Chapter Three: This chapter explains the end-to-end flow control in NoC and it goes through the CTC protocol specification and shows its main differences with respect to the normal CB protocol.

Chapter Four: This chapter demonstrates all the design details of a basic mesh-topology NoC using HDL and explains the construction of its verification environment. It also shows the design details of the network interfaces, implementing CTC and CB end-to-end flow control protocols.

Chapter Five: In this chapter, the NoC performance is evaluated using NoC standard traffic patterns, where the CTC performance is compared against normal CB protocol performance. This chapter also introduces the post-synthesis implementation results of the NoC implementing CTC and CB protocols, in 40nm TSMC CMOS technology. Finally, the area-saving results are presented.

Chapter Six: This chapter ends the thesis by conclusions, summary and future work.